

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart 31st Norchip Conference : Vilnius, Lithuania, 11-12 November 2013 : conference program and papers 2013 / p. 1-6 : ill [USB]

Bringing research issues into lab scenarios on the example of SoC testing [Electronic resource]

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<http://icee2007.dei.uc.pt/proceedings/papers/429.pdf>

Functional self-test of high-performance pipe-lined signal processing architectures

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart Microprocessors and microsystems 2015 / p. 909-918 : ill <https://doi.org/10.1016/j.micpro.2014.11.002> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Parallel pseudo-exhaustive testing of array multipliers with data-controlled segmentation

Oyeniran, Adeboye Stephen; Azad, Siavoosh Payandeh; Ubar, Raimund-Johannes 2018 IEEE International Symposium on Circuits and Systems (ISCAS) : 27-30 May 2018, Florence, Italy : proceedings 2018 / 5 p.: ill
<https://doi.org/10.1109/ISCAS.2018.8350936> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Replication-based deterministic testing of 2-dimensional arrays with highly interrelated cells

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Self-testing of pipe-lined signal processing architectures at-speed

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A tool set for teaching design-for-testability of digital circuits

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