Gate-level modelling of NBTI-induced delays under process variations
Copetti, Thiago; Cardoso Medeiros, Guilherme; Bolzani Poehls, Leticia; Vargas, Fabian; **Kostin, Sergei**; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 75-80 : ill http://dx.doi.org/10.1109/LATW.2016.7483343

Hierarchical identification of NBTI-critical gates in nanoscale logic
Kostin, Sergei; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

SPICE-inspired fast gate-level computation of NBTI-induced delays in nanoscale logic
Kostin, Sergei; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 223-228 : ill