

New fault models and self-test generation for microprocessors using High-Level Decision Diagrams

Jasnetski, Artjom; **Raik, Jaan**; Tšertov, Anton; Ubar, Raimund-Johannes 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 251-254 : ill

NoCDepend : a flexible and scalable dependability technique for 3D networks-on-chip

Hollstein, Thomas; **Azad, Siavoosh Payandeh**; Kogge, Thilo; Ying, Haoyuan; Hofmann, Klaus 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 75-78 : ill <http://dx.doi.org/10.1109/DDECS.2015.30>

SPICE-inspired fast gate-level computation of NBTI-induced delays in nanoscale logic

Kostin, Sergei; **Raik, Jaan**; Ubar, Raimund-Johannes; **Jenihhin, Maksim** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 223-228 : ill

SystemC-based loose models for simulation speed-up by abstraction of RTL IP cores

Abrar, Syed Saif; **Jenihhin, Maksim**; **Raik, Jaan** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 71-74 : ill
<http://dx.doi.org/10.1109/DDECS.2015.39>