

**Accurate NBTI-induced gate delay modeling based on intensive SPICE simulations**

**Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 21-26 : ill

**BASTION - board and SoC test instrumentation for Ageing and No Failure Found**

**Devadze, Sergei** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 77

**Decision diagrams for diagnostic modeling**

**Ubar, Raimund-Johannes** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 43

**A framework for area-efficient concurrent online checkers design**

**Saltarelli, Pietro; Niazmand, Behrad; Hariharan, Ranganathan; Raik, Jaan; Jervan, Gert; Hollstein, Thomas** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 64-69 : ill

**Integrated modelling, fault management, verification and reliable design environment for cyber-physical systems**

**Raik, Jaan; Rauwerda, Gerard; Zhao, Yong; Shibin, Konstantin** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 74