

A new testability calculation method to guide RTL test generation

Raik, Jaan; Nõmmeots, Tanel; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2005 / p. 71-82 : ill <https://doi.org/10.1007/s10836-005-5288-5>

A PC-based CAD system for training digital test

Ubar, Raimund-Johannes; Buldas, Ahto; Paomets, Priidu; Raik, Jaan; Tulit, Viljar The Fifth EUROCHIP Workshop on VLSI Design Training, 17-18-19 October 1994, Dresden, Germany 1994 / p. 152-157: ill

A scalable model based RTL framework zamiaCAD for static analysis

Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Tihhomirov, Valentin 2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC) : October 7-10, 2012 Santa Cruz, USA Dream Inn, Santa Cruz, USA : [proceedings] 2012 / p. 171-176 : ill <https://www.semanticscholar.org/paper/A-scalable-model-based-RTL-framework-zamiaCAD-for-Tsepurov-Bartsch/d19eefa44f793621d537c06498784e06e0332fd2>

A scalable static test set compaction method for sequential circuits

Aleksejev, Igor; Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 87-92 : ill

A synthesis-agnostic behavioral fault model for high gate-level fault coverage

Karputkin, Anton; Raik, Jaan 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2016 / p. 1124-1127 : ill <https://ieeexplore.ieee.org/document/7459477/figures#figures>

About robustness of test patterns regarding multiple faults

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / p. 86-91 : ill <https://www.infona.pl/resource/bwmeta1.element.ieee-art-000006261243>

Abstraction of clock interface for conversion of RTL VHDL to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan 2014 IEEE International Advance Computing Conference (IACC) : February 21-22, 2014, Gurgaon, India 2014 / p. 50-55 : ill

Accelerating transient fault injection campaigns by using Dynamic HDL Slicing

Bagbaba, Ahmet Cagri; Jenihhin, Maksim; Raik, Jaan; Sauer, Christian 2019 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC), 29-30 October 2019, Helsinki, Finland : proceedings in IEEE Xplore 2019 / 7 p. : ill <https://doi.org/10.1109/NORCHIP.2019.8906932>

Accurate NBTI-induced gate delay modeling based on intensive SPICE simulations

Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 21-26 : ill

AdAM: Adaptive Approximate Multiplier for Fault Tolerance in DNN Accelerators

Taheri, Mahdi; Cherezova, Natalia; Nazari, Samira; Azarpeyvand, Ali; Ghasempouri, Tara; Daneshtalab, Masoud; Raik, Jaan; Jenihhin, Maksim IEEE transactions on device and materials reliability 2024 / p. 66-75 : ill <https://doi.org/10.1109/TDMR.2024.3523386>

AdAM: adaptive fault-tolerant approximate multiplier for edge DNN accelerators

Taheri, Mahdi; Cherezova, Natalia; Nazari, Samira; Rafiq, Ahsan; Azarpeyvand, Ali; Ghasempouri, Tara; Daneshtalab, Masoud; Raik, Jaan; Jenihhin, Maksim 2024 IEEE European Test Symposium (ETS): ETS 2024 : May 20-24, 2024, The Hague, Netherlands : proceedings 2024 <https://doi.org/10.1109/ETS61313.2024.10567161> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Adaptive Kalman filter based data aggregation in fault-resilient Underwater Sensor Networks

Vihman, Lauri; Raik, Jaan 2023 24th International Conference on Digital Signal Processing (DSP) 2023 / p. 1-5 <https://doi.org/10.1109/DSP58604.2023.10167982>

ADAssure : debugging methodology for autonomous driving control algorithms

Roberts, Andrew James; Heidari Iman, Mohammad Reza; Bellone, Mauro; Ghasempouri, Tara; Raik, Jaan; Maennel, Olaf Manuel; Hamad, Mohammad; Steinhorst, Sebastian 2024 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2024 / p. 1-6 <https://doi.org/10.23919/DATE58400.2024.10546519>

Adjustable self-healing methodology for accelerated functions in heterogeneous systems

Riazati, Mohammad; Ghasempouri, Tara; Daneshtalab, Masoud; Raik, Jaan; Sjodin, Mikael; Lisper, Bjorn 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / p. 638-645 <https://doi.org/10.1109/DSD51259.2020.00104>

Advanced technical education in the age of cyber physical systems

Vierhaus, Heinrich Theodor; Schölzel, Mario; Raik, Jaan; Ubar, Raimund-Johannes 10th European Workshop on Microelectronics Education : EWME 2014 : May 14-16, 2014, Tallinn, Estonia 2014 / p. 193-198 : ill

Algorithms for hierarchical fault simulation in digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Klüver, B. Proceedings of the 10th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2003 : Lodz, Poland, 26-28 June 2003 2003 / p. 530-535 : ill

Algorithms for online CO2 baseline correction in intermittently occupied rooms

Vihman, Lauri; Parts, Tuule Mall; Aljas, Hans Kristjan; Thalfeldt, Martin; Raik, Jaan Healthy Buildings 2023 Europe: Beyond Disciplinary Boundaries: proceedings ; 1 2023 / p. 302-309 : ill <https://www.proceedings.com/content/070/070278webtoc.pdf>

An Accelerator-based architecture utilizing an efficient memory link for modern computational requirements

Yousefzadeh, Saba; Basharkhah, Katayoon; **Raik, Jaan; Jenihhin, Maksim** 2019 IEEE East-West Design & Test Symposium (EWDTS) 2019 / 6 p. : ill <https://doi.org/10.1109/EWDTS.2019.8884481>

An approach for PSL assertion coverage analysis with high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Shchenova, Tatjana Proceedings of IEEE East-West Design & Test Symposium (EWDTS'10) : St. Petersburg, Russia, September 17-20, 2010 2010 / p. 13-16 : ill <https://ieeexplore.ieee.org/document/5742048>

An approach for verification assertions reuse in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Fujiwara, Hideo; **Ubar, Raimund-Johannes; Viilukas, Taavi** Digest of papers : IEEE 11th Workshop on RTL and High Level Testing : WRTL'T'10 : December 5-6, 2010, Shanghai, China 2010 / p. 107-110 : ill

An automatic approach to evaluate assertions' quality based on data-mining metrics

Ghasempouri, Tara; Niazmand, Behrad; Raik, Jaan Proceedings 2nd IEEE International Test Conference in Asia : ITC-Asia 2018, 15-17 August 2018, Harbin, China 2018 / p. 61-66 : ill <https://doi.org/10.1109/ITC-Asia.2018.00021>

An educational environment for digital testing : hardware, tools, and web-based runtime platform

Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes; Vislogubov, Vladislav Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 412-419 : ill https://www.researchgate.net/profile/Artur-Jutman/publication/220880167_An_Educational_Environment_for_Digital_Testing_Hardware_Tools_and_Web-Based_Runtime_Platform/links/02e7e53c3c71b0b2a7000000/An-Educational-Environment-for-Digital-Testing-Hardware-Tools-and-Web-Based-Runtime-Platform.pdf

An external test approach for network-on-a-chip switches

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes ATS '06 : Proceedings of the 15th Asian Test Symposium : November 20-23, 2006, Fukuoka, Japan 2006 / p. 437-442 : ill <http://dx.doi.org/10.1109/ATS.2006.23>

An external test approach for network-on-a-chip switches

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 185-190 : ill

An XML-based test development and deployment framework for mixed-signal and digital devices

Mellik, Andres; Raik, Jaan 2008 IEEE AUTOTESTCON. Vols. 1 and 2 2008 / p. 193-196

Analysis and improvement of resilience for long short-term memory neural networks

Ahmadilivani, Mohammad Hasan; Raik, Jaan; Daneshtalab, Masoud; Kuusik, Alar 2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2023 / 4 p <https://doi.org/10.1109/DFT59622.2023.10313559>

Application of high-level decision diagrams for simulation-based verification tasks

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Estonian journal of engineering 2010 / 1, p. 56-77 : ill

Application of sequential test set compaction to LFSR reseeding

Aleksejev, Igor; Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes 26th Norchip Conference : Tallinn, Estonia, 17-18 November 2008 : formal proceedings 2008 / p. 102-107 : ill <http://dx.doi.org/10.1109/NORCHIP.2008.4738292>

Application specific true critical paths identification in sequential circuits

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan; Devadze, Sergei; Oyeniran, Adeboye Stephen 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 299-304 : ill <https://doi.org/10.1109/IOLTS.2019.8854442>

Applications of the open source HW design framework zamiaCAD

Tšepurov, Anton; Tihhomirov, Valentin; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p

APPRAISER : DNN fault resilience analysis employing approximation errors

Taheri, Mahdi; Ahmadilivani, Mohammad Hasan; Jenihhin, Maksim; Daneshtalab, Masoud; Raik, Jaan 2023 26th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) 2023 / p. 124–127 : ill
<https://ddecs2023.taltech.ee/> <https://doi.org/10.1109/DDECS57882.2023.10139468>

An approach for verification assertions reuse 2 in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Fujiwara, Hideo Journal of Shanghai Normal University : Natural Sciences 2010 / p. 441-447 : ill
https://www.researchgate.net/publication/240613999_An_Approach_for_Verification_Assertions_Reuse_in_RTL_Test_Pattern_Generation

Approaches to extra-functional verification of security and reliability aspects in hardware designs = Riistvaraprojektide turva- ja töökindlusaspektide ekstrasfunktsionaalse verifitseerimise lähenemisviisid

Lai, Xinhui 2022 <https://doi.org/10.23658/taltech.29/2022> <https://digikogu.taltech.ee/et/Item/cff1aeb9-b0b2-49ce-b81a-bfb9dc25fd56>
https://www.ester.ee/record=b5502807*est

APRICOT : a framework for teaching digital systems verification

Raik, Jaan; Jenihhin, Maksim; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes 19th EAAEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 172-177 : ill
<http://dx.doi.org/10.1109/EAAEIE.2008.4610181>

Arvutiteadlased: USA kiibipiirang lööb Eesti digiarengul hinge kinni

novaator.err.ee 2025 [Arvutiteadlased: USA kiibipiirang lööb Eesti digiarengul hinge kinni](#)

Assembling low-level tests to high-level symbolic test frames

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings [of the] 15th NORCHIP Conference, Tallinn, 10-11 November 1997 1997 / p. 275-280: ill

Assertion checking with PSL and high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Digest of papers IEEE 8th Workshop on RTL and High Level Testing : WRTL'07 : October 12-13, 2007, Beijing, China 2007 / p. 105-110 : ill
https://pld.ttu.ee/~maksim/phd_papers/%5B12%5D%20wrtl%2707.pdf

Assessment and Enhancement of Hardware Reliability for Deep Neural Networks = Riistvara töökindluse hindamine ja täiustamine süvanärvivõrkude jaoks

Ahmadilivani, Mohammad Hasan 2025 https://www.ester.ee/record=b5739227*est <https://digikogu.taltech.ee/et/Item/652d50e3-773f-4de5-897d-86531feb0d56> <https://doi.org/10.23658/taltech.19/2025>

Assessment of diagnostic test for automated bug localization

Tihhomirov, Valentin; Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [6] p. : ill

Assessment of electroencephalographic measures applied in the detection of depression = Depressiooni avastamiseks kasutatavate elektroentsefalograafilise signaali mõõdikute analüüs

Päeske, Laura 2021 https://www.ester.ee/record=b5411747*est <https://digikogu.taltech.ee/et/Item/44751b09-b47f-4757-847f-dd0f1d39b91b>
<https://doi.org/10.23658/taltech.17/2021>

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart 31st Norchip Conference : Vilnius, Lithuania, 11-12 November 2013 : conference program and papers 2013 / p. 1-6 : ill [USB]

Automated area and coverage optimization of minimal latency checkers

Azad, Siavoosh Payandeh; Niazmand, Behrad; Apneet Kaur; Raik, Jaan; Jervan, Gert; Hollstein, Thomas 2017 22nd IEEE European Test Symposium (ETS 2017), Limassol, Cyprus, 22 – 26 May 2017 : proceedings 2017 / p. 7-8 : ill
<https://doi.org/10.1109/ETS.2017.7968211>

Automated correction of design errors by edge redirection on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan 13th International Symposium on Quality Electronic Design (ISQED), 2012 2012 / p. 686-693 : ill <https://ieeexplore.ieee.org/document/6113980>

Automated design error debug using high-level decision diagrams and mutation operators

Raik, Jaan; Repinski, Urmas; Tšepurov, Anton; Hantson, Hanno; Ubar, Raimund-Johannes; Jenihhin, Maksim Microprocessors and microsystems 2013 / p. 505-513 : ill <https://doi.org/10.1016/j.micpro.2012.11.004> [Journal metrics at Scopus Article at Scopus](#) [Journal metrics at WOS Article at WOS](#)

Automated design error localization in RTL designs

Jenihhin, Maksim; Tšepurov, Anton; Tihhomirov, Valentin; Raik, Jaan; Hantson, Hanno; Ubar, Raimund-Johannes; Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich IEEE design & test of computers 2014 / p. 83-92 : ill

An automated method for mining high-quality assertion sets

Heidari Iman, Mohammad Reza; Raik, Jaan; Jenihhin, Maksim; Jervan, Gert; Ghasempouri, Tara Microprocessors and microsystems 2023 / art. 104773 <https://doi.org/10.1016/j.micpro.2023.104773> Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Automated minimization of concurrent online checkers for network-on-chips

Saltarelli, Pietro; Niazmand, Behrad; Hariharan, Ranganathan; Raik, Jaan; Jervan, Gert; Hollstein, Thomas 10th International Symposium on Reconfigurable and Communication-centric Systems-on-Chip (ReCoSoC 2015) : Bremen, 29 June - 1 July 2015 2015 / [8] p. : ill <http://dx.doi.org/10.1109/ReCoSoC.2015.7238079>

Automated test bench generation for high-level synthesis flow ABELITE

Viilukas, Taavi; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Baranov, Samary Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2011) : Sevastopol, Ukraine, September 9-12, 2011 2011 / p. 13-16 : ill <https://ieeexplore.ieee.org/document/6116601>

Automated test pattern generator with constraint solver

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 33-36

Automatic generation of EFSMs and HLDDs for functional ATPG

Tšepurov, Anton; Guglielmo, Giuseppe di; Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 143-146 : ill

Automatic test generation system for VLSI

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the First Electronic Circuits and Systems Conference : Bratislava, Slovakia, September 4-5, 1997 1997 / p. 255-258

AWAIT : an ultra-lightweight soft-error mitigation mechanism for network-on-chip links

Janson, Karl; Pihlak, Rene; Azad, Siavoosh Payandeh; Niazmand, Behrad; Jervan, Gert; Raik, Jaan 2018 13th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), Lille, France, July 9th-11th, 2018 2018 / p. 1-6 : ill <https://doi.org/10.1109/ReCoSoC.2018.8449374>

Back-tracing and event-driven techniques in high-level simulation with decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Morawiec, Adam ISCAS 2000 Geneva : The 2000 IEEE International Symposium on Circuits and Systems : Emerging Technologies for the 21st Century : May 28-31, 2000 : proceedings. Vol. 1 2000 / p. I-208 - I-211 <https://ieeexplore.ieee.org/document/857064>

BASTION : board and SoC test instrumentation for ageing and no failure found

Jutman, Artur; Lotz, Christophe; Larsson, Erik; Sonza Reorda, Matteo; Jenihhin, Maksim; Raik, Jaan Proceedings of the 2017 Design, Automation & Test in Europe (DATE) : 27-31 March 2017, Swisstech, Lausanne, Switzerland 2017 / p. 115-120 : ill <https://doi.org/10.23919/DATE.2017.7926968>

Block-level fault model-free debug and diagnosis in digital systems

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan Proceedings of the 12th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools : Patras, Greece, August 27-29, 2009 2009 / p. 229-232 <https://ieeexplore.ieee.org/document/5350128>

Built-in self diagnosis with multiple signature analyzers in digital systems

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 29-34 : ill

CAD software for digital test and diagnostics

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of International Conference on Design and Diagnostics of Electronic Circuits and Systems, Ostrava, Czech Republik, May 12-14, 1997 1997 / p. 35-40

A CAD system for teaching digital test

Ubar, Raimund-Johannes; Ivask, Eero; Paomets, Priidu; Raik, Jaan BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 369-372: ill

Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Microprocessors and microsystems 2020 / art. 103117, 12 p <https://doi.org/10.1016/j.micpro.2020.103117> Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Calculation of testability measures on structurally synthesized binary decision diagrams

Ubar, Raimund-Johannes; Heinlaid, J.; Raik, Jaan; Raun, L. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 179-182: ill

Calculation of the diagnosability of digital circuits without using fault models

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 159-162 : ill

Canonical representations of high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Raik, Jaan; Tombak, Mati Estonian journal of engineering 2010 / 1, p. 39-55 : ill

CLD : an accurate, cost-effective and scalable run-time Cache Leakage Detector

Shalabi, Ameer; Ghasempouri, Tara; Ellervee, Peeter; Raik, Jaan 2021 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : Vienna, Austria, 07-09 April 2021 / p. 127-132 : ill
<https://doi.org/10.1109/DDECS52668.2021.9417071>

Code coverage analysis for concurrent programming languages using high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes Proceedings of the 12th European Workshop on Dependable Computing : EWDC 2009 : Toulouse, France, May 14-15, 2009 / [4] p. : ill
<https://hal.archives-ouvertes.fr/hal-00381559>

Code coverage analysis using high-level decision diagrams [Electronic resource]

Raik, Jaan; Reinsalu, Uljana; Ubar, Raimund-Johannes; Jenihhin, Maksim; Ellervee, Peeter 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 / p. 201-207 : ill. [CD-ROM]
<https://ieeexplore.ieee.org/document/4538786>

Combined fault-model free cause-effect and effect-cause fault diagnosis in block-level digital networks

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan ASQED'09 : 1st Asia Symposium on Quality Electronic Design : Kuala Lumpur, Malaysia, July 15-16, 2009 / p. 385-390
<https://ieeexplore.ieee.org/document/5206232>

Combining dynamic slicing and mutation operators for ESL correction

Repinski, Urmass; Hantson, Hanno; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th-June 1st, 2012, Annecy, France 2012 / [6] p. : ill
<https://ieeexplore.ieee.org/document/6233020>

Combining learning, training and research in laboratory course for design and test

Ubar, Raimund-Johannes; Orasson, Elmet; Raik, Jaan; Wuttke, Heinz-Dietrich The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 221-224 : ill
https://www.researchgate.net/publication/242397131_Combining_Learning_Training_and_Research_in_Laboratory_Course_for_Design_and_Test

Comparative analysis of sequential circuit test generation approaches

Raik, Jaan; Krivenko, Anna; Ubar, Raimund-Johannes BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 225-228 : ill

Comparative mixed-signal test method and toolset

Mellik, Andres; Raik, Jaan IEEE International Workshop on Open Source Test Technology Tools (IOST3) 2007 / ? p

Comparison of genetic and random techniques for test pattern generation

Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 163-166: ill

Comparison of model-based error localization algorithms for C designs

Repinski, Urmass; Raik, Jaan Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14-17, 2012 / p. 42-45
<https://ieeexplore.ieee.org/document/6673203>

Comprehensive abstraction of VHDL RTL cores to ESL SystemC = Register-siirde taseme VHDL kirjelduste kompleksne abstraherimine süsteemitaseme SystemC mudeliteks

Abrar, Syed Saif 2016 http://www.ester.ee/record=b4564850*est

Comprehensive performance and robustness analysis of 2D turn models for network-on-chips

Azad, Siavoosh Payandeh; Niazmand, Behrad; Janson, Karl; Kogge, Thilo; Raik, Jaan; Jervan, Gert; Hollstein, Thomas 2017 IEEE International Symposium on Circuits and Systems (ISCAS) 2017 / p. 1476-1479 : ill
<https://doi.org/10.1109/ISCAS.2017.8050634> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Computer scientists: Estonia's digital development held back by US chip limit

news.err.ee 2025 [Computer scientists: Estonia's digital development held back by US chip limit](#)

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Raik, Jaan; Rannaste, Anna; Jenihhin, Maksim; Viilukas, Taavi; Ubar, Raimund-Johannes; Fujiwara, Hideo Sixteenth IEEE European Test Symposium : 23-27 May 2011, Trondheim 2011 / p. 147-152

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Viilukas, Taavi; Raik, Jaan; Ubar, Raimund-Johannes; Rannaste, Anna; Jenihhin, Maksim; Fujiwara, Hideo Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 139-142 : ill

Constraint-based test pattern generation at the register-transfer level

Viilukas, Taavi; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Krivenko, Anna Proceedings of the 13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 14-16, 2010, Vienna, Austria 2010 / p. 352-357 : ill <http://dx.doi.org/10.1109/DDECS.2010.5491752>

A constraint-driven gate-level test generator

Raik, Jaan; Ubar, Raimund-Johannes; Jervan, Gert; Krupnova, Helena BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 237-240: ill

Constraints solving based hierarchical test generation for synchronous sequential circuits = Kitsenduste lahendamisel baseeruv hierarhiline testigeneerimine sünkroonsetele järjestiksskeemidele

Viilukas, Taavi 2012 https://www.ester.ee/record=b2888278*est

Cost-effective concurrent hardware checkers for network on chip based system on chip = Kulutõhusad süsteemiga paralleelsed rikkemonitorid kiipvõrkudel põhinevatele kiipsüsteemidele

Hariharan, Ranganathan 2019 <https://digi.lib.ttu.ee/i/?12854> https://www.ester.ee/record=b5243161*est

Cost-effective fault tolerance for CNNs using parameter vulnerability based hardening and pruning

Ahmadilivani, Mohammad Hasan; Mousavi, Seyedhamidreza; Raik, Jaan; Daneshtalab, Masoud; Jenihhin, Maksim 2024 IEEE 30th International Symposium on On-line Testing and Robust System Design (IOLTS) : IOLTS 2024 : July 03rd-05th 2024, Rennes, Brittany, France 2024 / 7 p <https://doi.org/10.1109/IOLTS60994.2024.10616072> [Article at Scopus](#) [Article at WOS](#)

Critical path tracing based simulation of transition delay faults

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 61-66 : ill

Critical path tracing based simulation of transition delay faults

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 108-113 : ill

Cross-layer dependability management in network on chip based system on chip = Kiipvõrkudel põhinevate süsteemide kihtideülene usaldatavuse haldus

Azad, Siavoosh Payandeh 2018 <https://digi.lib.ttu.ee/i/?9948> https://www.ester.ee/record=b5056143*est

Cycle-based simulation algorithms for digital systems using high-level decision diagrams

Morawiec, Adam; Ubar, Raimund-Johannes; Raik, Jaan Design, Automation and Test in Europe : Conference and Exhibition 2000 : Paris, France, March 27-30, 2000 : proceedings 2000 / p. 743 <https://ieeexplore.ieee.org/document/840876>

Cycle-based simulation with decision diagrams

Ubar, Raimund-Johannes; Morawiec, Adam; Raik, Jaan Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 454-458: ill <https://ieeexplore.ieee.org/document/761165>

Data-driven cross-layer fault management architecture for sensor networks

Vihman, Lauri; Kruusmaa, Maarja; Raik, Jaan 16th European Dependable Computing Conference : EDCC 2020 : Virtual Conference, Munich, Germany, 7-10 September 2020 : proceedings 2020 / art. 20094188, p. 33-40 <https://doi.org/10.1109/EDCC51268.2020.00015>

Data-driven fault-resilient cross-layer sensor network architecture = Andmepõhine tõrkekindel kihtideülene sensorvõrgu arhitektuur

Vihman, Lauri 2024 https://www.ester.ee/record=b5657135*est <https://digikogu.taltech.ee/et/Item/00a93258-dc0f-4a4d-822f-099fff757224> <https://doi.org/10.23658/taltech.7/2024>

DECIDER : a decision diagram based hierarchical test generation system

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 2nd International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Szczyrk, Poland, September 2-4, 1998 1998 / p. 269-273
<https://www.ida.liu.se/labs/eslab/publications/pap/db/DDECS98.pdf>

DECIDER : a system for hierarchical test pattern generation

Raik, Jaan; Ubar, Raimund-Johannes Radioelectronics and informatics 2003 / p. 40-45 : ill
https://www.researchgate.net/publication/250395975_DECIDER_A_System_for_Hierarchical_Test_Pattern_Generation

A decision diagram based hierarchical test pattern generator

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 159-162: ill

Deductive fault simulation on structurally synthesized BDDs

Aarna, Margit; Ubar, Raimund-Johannes; Raik, Jaan BEC 2004 : Baltic Electronics Conference : Post-Graduate Student Session : Tallinn University of Technology, October 3-6, 2004, Tallinn, Estonia 2004 / p. 11 : ill

DeepAxe : a framework for exploration of approximation and reliability trade-offs in DNN accelerators

Taheri, Mahdi; Riazati, Mohamad; Ahmadiilivani, Mohammad Hasan; Jenihhin, Maksim; Daneshtalab, Masoud; Raik, Jaan; Sjödin, Mikael; Lisper, Björn 2023 24th International Symposium on Quality Electronic Design (ISQED) 2023 / 8 p. : ill
<https://doi.org/10.1109/ISQED57927.2023.10129353>

DeepVigor: Vulnerability Value RanGes and FactORs for DNNs' Reliability Assessment

Ahmadiilivani, Mohammad Hasan; Taheri, Mahdi; Raik, Jaan; Daneshtalab, Masoud; Jenihhin, Maksim IEEE European Test Symposium (ETS) : Venice, Italy, 22-26 May 2023 : proceedings 2023 / 6 p. : ill <https://doi.org/10.1109/ETS56758.2023.10174133>

DeepVigor+: Scalable and Accurate Semi-Analytical Fault Resilience Analysis for Deep Neural Networks

Ahmadiilivani, Mohammad Hasan; Raik, Jaan; Daneshtalab, Masoud; Jenihhin, Maksim arXiv.org 2024 / 14 p. : ill
<https://doi.org/10.48550/arXiv.2410.15742>

Defect oriented fault coverage of 100stuck-at fault test sets

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 7th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2000 : Gdynia, Poland, 15-17 June 2000 2000 / p. 511-516 : ill <https://repo.pw.edu.pl/info/seam?ps=20&id=WUT7e20f35d67ae45d3b2d1264d7a4ba722&en&pn=1&cid=156607>

Defect-oriented BIST quality analysis

Kruus, Helena; Ubar, Raimund-Johannes; Raik, Jaan BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 153-156 : ill

Defect-oriented fault simulation and test generation in digital circuits

Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE ISQED 2001 : proceedings of the IEEE 2001 2nd International Symposium on Quality Electronic Design : March 26-28, 2001, San Jose, California 2001 / p. 365-371
<https://ieeexplore.ieee.org/document/915257>

Defect-oriented library builder and hierarchical test generation

Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Győr, Hungary, April 18-20, 2001 2001 / p. 163-168 : ill

Defect-oriented mixed-level fault simulation in digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina Facta Universitatis [Niš]. Series electronics and energetics 2002 / 1, April, p. 123-136 : ill

Defect-oriented modul-level fault diagnosis in digital circuits

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 81-86

Defect-oriented test- and layout-generation for standard-cell ASIC designs

Sudbrock, Joachim; **Raik, Jaan; Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw; Pleskacz, Witold A. Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 79-82 : ill <https://ieeexplore.ieee.org/document/1559781>

Defect-oriented test generation using probabilistic estimation

Cibakova, Tatiana; Fischerova, Maria; Gramatova, Elena; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 131-136 : ill

Dependability evaluation in fault-tolerant systems with high-level decision diagrams

Ubar, Raimund-Johannes; Jervan, Gert; Raik, Jaan; Jenihhin, Maksim; Ellervee, Peeter Computer Science Meets Automation : 10-13 September 2007 : proceedings. Volume II 2007 / p. 147-152 : ill https://www.db-thueringen.de/receive/dbt_mods_00008864

Dependability improvements of NoC-based systems = Töökindluse parandamine kiipvõrkudel põhinevates süsteemides

Niazmand, Behrad 2018 <https://digi.lib.ttu.ee/i/79879> https://www.ester.ee/record=b4907650*est

Dependence of the EEG nonlinear coupling on the frequency bands and the segment lengths

Orgo, Laura; Bachmann, Maie; Kalev, Kaia; Järvelaid, Mari; Raik, Jaan; Hinrikus, Hiie EMBEC & NBC 2017 : joint conference of the European Medical and Biological Engineering Conference (EMBEC) and the Nordic-Baltic Conference on Biomedical Engineering and Medical Physics (NBC), Tampere, Finland, June 2017 2018 / p. 799-802 https://doi.org/10.1007/978-981-10-5122-7_200 [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Design and test technology for dependable systems-on-chip

2011 https://www.ester.ee/record=b4467408*est

Design error diagnosis using backtrace algorithm on decision diagrams

Repinski, Urmas; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

Design space exploration of SABER in 65nm ASIC

Imran, Malik; Almeida, Felipe; Raik, Jaan; Basso, Andrea; Roy, Sujoy Sinha; Pagliarini, Samuel Nascimento ASHES '21 : proceedings of the 5th Workshop on Attacks and Solutions in Hardware Security 2021 / p. 85-90 <https://doi.org/10.1145/3474376.3487278>

Design understanding : from logic to specification

Fey, Goerschwin; Ghasempouri, Tara; Jacobs, Swen; Raik, Jaan Proceedings of the 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 8-10, 2018, Verona, Italy 2018 / p. 172-175 : ill <https://doi.org/10.1109/VLSI-SoC.2018.8644732>

Design-for-destability-based external test and diagnosis of mesh-like network- on-a-chips

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes IET computers and digital techniques 2009 / 5, p. 476-486 : ill <http://dx.doi.org/10.1049/iet-cdt.2008.0096>

Design-for-testability for application of external test patterns in a NoC

Govind, Vineeth; Raik, Jaan 2nd Workshop on Diagnostic Services in Network-on-Chips - Test, Debug, and On-Line Monitoring, in conjunction with Design Automation Conference (DAC) 2008 / [4] p

Designing reliable cyber-physical systems

Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; Devadze, Sergei; Jenihhin, Maksim; Jutman, Artur; Raik, Jaan; Shibin, Konstantin Languages, design methods, and tools for electronic system design : selected contributions from FDL 2016 2018 / p. 15-38 : ill https://doi.org/10.1007/978-3-319-62920-9_2 [Conference Proceedings at Scopus](#) [Article at Scopus](#)

Designing reliable cyber-physical systems : overview associated to the special session at FDL'16

Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; Devadze, Sergei; Jenihhin, Maksim; Jutman, Artur; Raik, Jaan; Shibin, Konstantin The 2016 Forum on Specification & Design Languages : proceedings : Bremen, Germany, September 14-16, 2016 2016 / [8] p. : ill <https://doi.org/10.1109/FDL.2016.7880382>

Deterministic defect-oriented test generation for combinational circuits

Raik, Jaan; Ubar, Raimund-Johannes; Sudbrock, Joachim; Kuzmich, Wieslaw; Pleskacz, Witold A. LATW 2005 : 6th IEEE Latin-American Test Workshop : March 30 - April 2, 2005, Salvador, Bahia, Brazil : [digest of papers] 2005 / p. 325-330 : ill

DfT for application of external test patterns in a Network-on-a-Chip

Govind, Vineeth; Raik, Jaan; Ubar, Raimund-Johannes Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 25-28 : ill

DfT-based external test and diagnosis of mesh-like networks on chips = Testitavusel põhinev välise testi ja diagnoosi meetod kahemõõtmelistele kiipvõrkudele

Govind, Vineeth 2009 <https://digi.lib.ttu.ee/i/7454> https://www.ester.ee/record=b2539211*est

Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis

Hantson, Hanno; Repinski, Urmas; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / [6 p.] : ill <https://ieeexplore.ieee.org/document/6261234>

Diagnostic modeling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill https://www.researchgate.net/publication/344994231_Diagnostic_Modeling_of_Digital_Systems_with_Multi-Level_Decision_Diagrams

Diagnostic modeling of microprocessors with high-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Brik, Marina; Istenberg, Martin; Wuttke, Heinz-Dietrich BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 147-150 : ill

Diagnostic modelling of digital systems with binary and high-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Kruus, Helena; Lensen, Harri; Evartson, Teet Progress in industrial mathematics at ECMI 2006 2008 / p. 902-907 : ill https://link.springer.com/chapter/10.1007/978-3-540-71992-2_158

Diagnostic modelling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Evartson, Teet; Kruus, Margus; Lensen, Harri Proceedings of the 17th IASTED International Conference on Modelling and Simulation : May 24-26, 2006, Montreal, Quebec, Canada 2006 / p. 207-212 : ill

Diagnostic software with WEB interface for teaching purposes

Vislogubov, Vladislav; **Jutman, Artur; Kruus, Helena; Orasson, Elmet; Raik, Jaan; Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 255-258 : ill

Diagnostic test generation for statistical bug localization using evolutionary computation

Gaudesi, Marco; **Jenihhin, Maksim; Raik, Jaan; Tihomirov, Valentin; Ubar, Raimund-Johannes** Applications of Evolutionary Computation : 17th European Conference, EvoApplications 2014, Granada, Spain, April 23-25, 2014 : revised selected papers 2014 / p. 425-436 : ill https://doi.org/10.1007/978-3-662-45523-4_35 [Conference proceeding at Scopus](#) [Article at Scopus](#) [Conference proceeding at WOS](#) [Article at WOS](#)

DIAGNOZER : a laboratory tool for teaching research in diagnosis of electronic systems [Electronic resource]

Ubar, Raimund-Johannes; Kostin, Sergei; Jutman, Artur; Raik, Jaan; Wuttke, Heinz-Dietrich 2009 IEEE International Conference on Microelectronic Systems Education MSE '09 : 25-27 July 2009, San Francisco, California : [proceedings] 2009 / p. 12-15 : ill. [CD-ROM] <http://dx.doi.org/10.1109/MSE.2009.5270842>

Digitaalkiipide projekteerimine ja test : teadus, tehnoloogia või kunst

Raik, Jaan A & A 2005 / lk. 5-9

Digital design flow with test activities

Diener, Karl-Heinz; Elst, G.; **Ivask, Eero; Jervan, Gert; Peng, Z.; Raik, Jaan; Ubar, Raimund-Johannes** VILAB User Forum 2000 / [11] p

Digital electronics design and test at Computer Engineering Department of Tallinn University of Technology

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Ellervee, Peeter The house magazine : the parliamentary weekly 2006 / 1198, p. 42 : ill

Digital logic simulation with compressed BDDs

Ubar, Raimund-Johannes; Mironov, Dmitri; Devadze, Sergei; Raik, Jaan Proceedings : 2011 IEEE International Conference on Computer Science and Automation Engineering : June 10-12, 2011, Shanghai, China 2011 / p. 105-109 : ill <https://ieeexplore.ieee.org/document/5952643>

Distributed approach for genetic test generation in the field of digital electronics

Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes Intelligent Distributed Computing, Systems and Applications : proceedings of the 2nd International Symposium on Intelligent Distributed Computing : IDC 2008 : Catania, Italy, 2008 2008 / p. 127-136

DOT: new deterministic defect-oriented ATPG tool

Raik, Jaan; Ubar, Raimund-Johannes; Sudbrock, Joachim; Kuzmicz, Wieslaw; Pleskacz, Witold A. European Test Symposium : ETS 2005 : 22-25 May 2005, Tallinn, Estonia : proceedings 2005 / p. 96-101 : ill

EEG functional connectivity detects seasonal changes

Päeske, Laura; Bachmann, Maie; Raik, Jaan; Hinrikus, Hiie World Congress on Medical Physics and Biomedical Engineering 2018 : June 3-8, 2018, Prague, Czech Republic (Vol. 2) 2018 / p. 237-240 https://doi.org/10.1007/978-981-10-9038-7_44 [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Eesti teadlased loodavad panna putukrobotile pähe tehisarv

Raik, Jaan novaator.err.ee 2024 [Eesti teadlased loodavad panna putukrobotile pähe tehisarv](#) [Эстонские ученые создают робота-насекомого с искусственным интеллектом](#)

Eesti teaduse nähtamatud hiiglased

Raik, Jaan Teadusmõte Eestis (X). Tehnikateadused. 3 : [artiklikogumik] 2019 / lk. 161-168 : ill., fot
https://www.ester.ee/record=b5208765*est

Eestisse luuakse kiibitehnoloogia kompetentsikeskus

Tambur, Silver Trialoog 2025 <https://trialoog.taltech.ee/eestisse-luuakse-kiibitehnoloogia-kompetentsikeskus/>

An efficient analog convolutional neural network hardware accelerator enabled by a novel memoryless architecture for insect-sized robots

Dadras, Iman; **Ahmadilivani, Mohammad Hasan**; Banerji, Saoni; **Raik, Jaan**; Abloo, Alvo 2022 11th International Conference on Modern Circuits and Systems Technologies (MOCASST) : Bremen, Germany : 08-10 June 2022 / p. 1-6
<https://doi.org/10.1109/MOCASST54814.2022.9837551>

Efficient fault injection based on dynamic HDL slicing technique

Bagbaba, Ahmet Cagri; **Jenihhin, Maksim**; **Raik, Jaan**; Sauer, Christian 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 52-53 : ill
<https://doi.org/10.1109/IOLTS.2019.8854419>

An efficient FPGA-based architecture for contractive autoencoders

Kerner, Madis; **Tammemäe, Kalle**; **Raik, Jaan**; Hollstein, Thomas 2020 IEEE 28th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 3 – 6 May 2020, Fayetteville, Arkansas : proceedings 2020 / p. 230-230
<https://doi.org/10.1109/FCCM48280.2020.00062>

Efficient hierarchical approach to test generation for digital systems

Ubar, Raimund-Johannes; **Raik, Jaan** IEEE ISQED 2000 : proceedings of the IEEE 2000 1st International Symposium on Quality Electronic Design : March 20-22, 2000, San Jose, California 2000 / p. 189-195 : ill <https://ieeexplore.ieee.org/document/838873>

Efficient single-pattern fault simulation on structurally synthesized BDDs

Raik, Jaan; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Jutman, Artur** Dependable Computing - EDCC-5 : 5th European Dependable Computing Conference : Budapest, Hungary, April 20-22, 2005 : proceedings 2005 / p. 332-344 : ill

E-learning environment for WEB-based study of testing

Ubar, Raimund-Johannes; **Jutman, Artur**; **Raik, Jaan**; **Devadze, Sergei**; **Jenihhin, Maksim**; **Aleksejev, Igor**; **Tšepurov, Anton**; **Tšertov, Anton**; **Kostin, Sergei**; **Orasson, Elmet**; Wuttke, Heinz-Dietrich Proceedings of the 8th European Workshop on Microelectronics Education : EWME 2010 : Darmstadt, Germany, 10-12 May 2010 / p. 47-52 : ill

Embedded diagnosis in digital systems

Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** 2008 26th International Conference on Microelectronics : Niš, Serbia, 11-14 May 2008 : proceedings. Vol. 2 2008 / p. 421-424 : ill

Embedded fault diagnosis in digital systems with BIST

Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Microprocessors and microsystems 2008 / 5/6, p. 279-287 : ill

Energy-efficient multi-fragment Markov model guided online model-based testing for MPSoC

Vain, Jüri; **Tsiopoulos, Leonidas**; Kharchenko, Vyacheslav; **Apneet Kaur**; **Jenihhin, Maksim**; **Raik, Jaan**; **Nömm, Sven** Green IT Engineering: Social, Business and Industrial Applications 2019 / p. 273-297 https://doi.org/10.1007/978-3-030-00253-4_12 [Article collection at Scopus](#) [Article at Scopus](#)

Engineering of an effective automatic dynamic assertion mining platform

Ghasempouri, Tara; Malburg, Jan; Danese, Alessandro; Pravadelli, Graziano; Fey, Goerschwin; **Raik, Jaan** VLSI-SoC 2019 : 27th IFIP/IEEE International Conference on Very Large Scale Integration : [proceedings] 2019 / p. 111-116 : ill <https://doi.org/10.1109/VLSI-SoC.2019.8920331>

Enhancing fault resilience of QNNs by selective neuron splitting

Ahmadilivani, Mohammad Hasan; **Taheri, Mahdi**; **Raik, Jaan**; **Daneshtalab, Masoud**; **Jenihhin, Maksim** 2023 IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS) 2023 / 5 p. : ill
<https://doi.org/10.1109/AICAS57966.2023.10168633>

Enhancing hierarchical ATPG with a functional fault model for multiplexers [Electronic resource]

Raik, Jaan; **Ubar, Raimund-Johannes** 7th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 18-21, 2004, Stará Lesná, Slovakia : proceedings 2004 / p. 219-222 : ill. [CD-ROM] <https://www.semanticscholar.org/paper/Enhancing-Hierarchical-Atpg-with-a-Functional-Fault-Raik-Ubar/b42e913ac070fd774df97bd644c4e6220704f8d4>

Environment for fault simulation acceleration on FPGA

Ellervee, Peeter; **Raik, Jaan**; Tihomirov, Valentin BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 217-220 : ill

Environment for FPGA-based fault emulation

Ellervee, Peeter; Raik, Jaan; Tammemäe, Kalle; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 2006 / 3-2, p. 323-335 : ill

Evaluating fault emulation on FPGA

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin; Tammemäe, Kalle Field-Programmable Logic and Applications : 14th International Conference, FPL 2004 : Antwerp, Belgium, August 30-September 1, 2004 : proceedings 2004 / p. 354-363 : ill
https://link.springer.com/chapter/10.1007/978-3-540-30117-2_37

Evolutionary approach to test generation for functional BIST

Skobtsov, Y.A.; Ivanov, D.E.; Skobtsov, V.Y.; Ubar, Raimund-Johannes; Raik, Jaan Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005 2005 / p. 151-155 : ill https://artiklid.elnet.ee/record=b1018764*est

Exact parallel critical path fault tracing to speed-up fault simulation in sequential circuits

Kõusaar, Jaak; Ubar, Raimund-Johannes; Kostin, Sergei; Devadze, Sergei; Raik, Jaan International journal of microelectronics and computer science 2018 / p. 9-18 <https://ijmcs.dmc.s.pl/web/guest/vol.-9-no.-1>
https://ijmcs.dmc.s.pl/documents/10630/345460/IJMCS_1_2018_2.pdf

Exact static compaction of independent test sequences

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 315-318 : ill

Exact static compaction of sequential circuit tests using branch-and-bound and search state registration

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes ETW'02 : 7th IEEE European Test Workshop, Gorfou Greece, May 26-29, 2002 : informal digest 2002 / p. 19-20
https://www.researchgate.net/publication/250423148_Exact_Static_Compaction_of_Sequential_Circuit_Tests_Using_Branch_and-Bound_and_Search_State_Registration

Experimental comparison of different diagnosis algorithms in the BIST environment

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan; Kruus, Margus Proceedings of the 16th IASTED International Conference on Applied Simulation and Modelling : August 29-31, 2007, Palma de Mallorca, Spain 2007 / p. 271-276 : ill
https://www.researchgate.net/publication/262275431_Experimental_comparison_of_different_diagnosis_algorithms_in_the_BIST_environment

Exploiting high-level descriptions for circuits fault tolerance assessments

Benso, A.; Prinetto, Paolo; Rebaudengo, M.; Sonza Reorda, Matteo; Raik, Jaan; Ubar, Raimund-Johannes 1997 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Paris, October 20-22, 1997 1997 / p. 212-216
<https://ieeexplore.ieee.org/document/628327>

Exploration of Activation Fault Reliability in Quantized Systolic Array-Based DNN Accelerators

Taheri, Mahdi; Cherezova, Natalia; Ansari, Mohammad Saeed; Jenihhin, Maksim; Mahani, Ali; Daneshtalab, Masoud; Raik, Jaan 25th International Symposium on Quality Electronic Design (ISQED) 2025 / 8 p. : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=10528372>

Explorations in low area overhead DfT techniques for sequential BIST

Raik, Jaan; Raidma, Rein; Ubar, Raimund-Johannes IEEE NORCHIP 2003 : 21 Norchip Conference : Riga, Latvia, 10-11 November 2003 : proceedings 2003 / p. 220-223 : ill

Extended checkers for control part of routers in network-on-chips

Hariharan, Ranganathan; Niazmand, Behrad; Hollstein, Thomas; Raik, Jaan; Jervan, Gert MEDIAN 2015 : the 4th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : March 13, 2015, Grenoble, France 2015 / p. 36-39 : ill

Extended checkers for logic-based distributed routing in network-on-chips

Niazmand, Behrad; Hariharan, Ranganathan; Govind, Vineeth; Jervan, Gert; Hollstein, Thomas; Raik, Jaan Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 83-86 : ill

Extended checkers for logic-based distributed routing in network-on-chips

Niazmand, Behrad; Hariharan, Ranganathan; Govind, Vineeth; Jervan, Gert; Hollstein, Thomas; Raik, Jaan BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 77-80 : ill

Extensible open-source framework for translating RTL VHDL IP cores to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

An external diagnosis method for network-on-a-chip

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes IEEE/ACM Design Automation and Test in Europe, Workshop on

Fast and efficient static compaction of test sequences based on greedy algorithms

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Győr, Hungary, April 18-20, 2001 2001 / p. 117-122 https://slideplayer.com/slide/9971880/#google_vignette

Fast and efficient static compaction of test sequences using bipartite graph representations

Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes ECS'99 : proceedings of the 2nd Electronic Circuits and Systems Conference : September 6-8, 1999, Bratislava, Slovakia 1999 / p. 17-20

Fast fault emulation for synchronous sequential circuits

Raik, Jaan; Ellervee, Peeter; Tihomirov, Valentin; Ubar, Raimund-Johannes Proceedings of East-West Design & Test Workshop (EWDWTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 35-40
<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=a6eb712498a5f23db3f95ad66bada257c21e96f0>

Fast fault simulation for extended class of faults in scan-path circuits

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur Proceedings : Fifth IEEE International Symposium on Electronic Design, Test and Applications : DELTA 2010 : 13-15 January 2010, Ho Chi Minh City, Vietnam 2010 / p. 14-19
<https://ieeexplore.ieee.org/document/5438717>

Fast identification of true critical paths in sequential circuits

Ubar, Raimund-Johannes; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan; Jürimägi, Lembit Microelectronics reliability 2018 / p. 252-261 : ill <https://doi.org/10.1016/j.microrel.2017.11.027> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast RTL fault simulation using decision diagrams and bitwise set operations

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes; Ellervee, Peeter 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 3-5 October 2011, Vancouver, Canada 2011 / p. 164-170
<https://ieeexplore.ieee.org/document/6104440>

Fast static compaction of test sequences using implications and greedy search

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes ETW 2001 : IEEE European Test Workshop : Stockholm, May 29 June 1, 2001 : informal digest 2001 / p. 207-209 : ill <https://www.semanticscholar.org/paper/Fast-Static-Compaction-of-Test-Sequences-using-and-Raik-Jutman/3a7a8ddda6e63d3e2fde0c8650d4518851746221>

Fast static compaction of tests composed of independent sequences : basic properties and comparison of methods

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes The 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS 2002 : September 15-18, 2002, Dubrovnik, Croatia. Volume II 2002 / p. 445-448 : ill
<http://dx.doi.org/10.1109/ICECS.2002.1046190> <https://ieeexplore.ieee.org/document/1046190>

Fast test pattern generation for sequential circuits using decision diagram representations

Raik, Jaan; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications (JETTA) 2000 / 3, p. 213-226 : ill
<https://link.springer.com/article/10.1023/A:1008335130158>

Fault collapsing in digital circuits using fast fault dominance and equivalence analysis with SSBDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; Orasson, Elmet; Raik, Jaan VLSI-SoC : Design for Reliability, Security, and Low Power : 23rd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2015 Daejeon, Korea, October 5-7, 2015 : revised selected papers 2016 / p. 23-45 : ill https://doi.org/10.1007/978-3-319-46097-0_2 [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Fault collapsing with linear complexity in digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS 2010) : 30 May - 2 June 2010, Paris, France 2010 / p. 653-656 : ill
<https://ieeexplore.ieee.org/document/5537504>

Fault diagnosis in integrated circuits with BIST

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan; Evertson, Teet; Lensen, Harri 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 604-610 : ill <http://dx.doi.org/10.1109/DSD.2007.4341530>

Fault diagnosis in the BIST environment based on bisection of detected faults

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan LATW2007 : 8th IEEE Latin-American Test Workshop : March 11-14, 2007, Cuzco, Peru 2007 / [6] p. : ill

Fault emulation on FPGA : a feasibility study

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin IEEE NORCHIP 2003 : 21 Norchip Conference : Riga, Latvia, 10-11 November

2003 : proceedings 2003 / p. 92-95 : ill https://www.researchgate.net/publication/246171898_Fault_Emulation_on_FPGA_A_Feasibility_Study

Fault model and test synthesis for RISC-processors

Ubar, Raimund-Johannes; Markus, Antti; Jervan, Gert; Raik, Jaan BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 229-232: ill

Fault oriented test pattern generation for sequential circuits using genetic algorithms

Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes IEEE European Test Workshop 2000 / p. 319-320

Fault oriented test pattern generation for sequential circuits using Genetic Algorithms

Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 129-132 : ill

Fault simulation and code coverage analysis of RTL designs using high-level decision diagrams = Rikete simuleerimine ja koodikatte analüüs register-siirde tasemel kasutades kõrgtaseme otsustusdiagramme

Reinsalu, Uljana 2013 https://www.ester.ee/record=b2963595*est

Fault simulation with parallel critical path tracing for combinational circuits using structurally synthesized BDDs

Devadze, Sergei; Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 97-102 : ill

Fault-aware performance assessment approach for embedded networks

Malburg, Jan; **Janson, Karl; Raik, Jaan; Dannemann, Frank** 2019 22nd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Cluj-Napoca, Romania : proceedings 2019 / 4 p. : ill
<https://doi.org/10.1109/DDECS.2019.8724670>

Fault-resilient NoC router with transparent resource allocation

Putkaradze, Tsotne; Azad, Siavoosh Payandeh; Niazmand, Behrad; Raik, Jaan; Jervan, Gert 12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC2017), July 12-14, 2017, Madrid, Spain : proceedings 2017 / 8 p. : ill <https://doi.org/10.1109/ReCoSoC.2017.8016161> <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8016161>

Feasibility of structurally synthesized BDD models for test generation

Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the IEEE European Test Workshop, Barcelona, Spain, May 27-29, 1998 1998 / p. 145-146

FoREnSiC– an automatic debugging environment for C programs

Bloem, Roderick; **Raik, Jaan; Repinski, Urmaz** Eighth Haifa Verification Conference : HVC 2012 : November 6-8, Haifa, Israel : [proceedings] 2013 / p. 260-265 : ill https://doi.org/10.1007/978-3-642-39611-3_24 [Conference Proceedings at Scopus](#) [Article at Scopus](#)

Formal verification and error correction on high-level decision diagrams = Formaalne verifitseerimine ja vigade parandamine kõrgtasemelistel otsustusdiagrammidel

Karputkin, Anton 2012

FP7 collaborative research project DIAMOND : diagnosis, error modeling and correction for reliable systems design

Raik, Jaan Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th–June 1st, 2012, Annecy, France 2012 / 1 p
<https://ieeexplore.ieee.org/document/6233052>

FP7 DIAMOND : design error diagnosis and correction success stories

Raik, Jaan; Jenihhin, Maksim; Könighofer, Robert European Test Symposium (ETS), 2013, Avignon, France 2013 / p. 1-6

FPGA based fault emulation of synchronous sequential circuits

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin; Ubar, Raimund-Johannes Proceedings [of] 22nd NORCHIP Conference : Oslo, Norway, 8-9 November 2004 2004 / p. 59-62 <https://ieeexplore.ieee.org/abstract/document/1423822>

FPGA design flow with automated test generation

Elst, G.; Diener, Karl-Heinz; **Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes** Proc. of German 11th Workshop on Test Technology and Reliability of Circuits and Systems : Potsdam, 1999 1999 / p. 120-123
<https://masters.donntu.ru/2010/fknt/masyakin/library/article7.pdf>

FPGA-based fault emulation of synchronous sequential circuits

Ellervee, Peeter; Raik, Jaan; Tammemäe, Kalle; Ubar, Raimund-Johannes IET computers and digital techniques 2007 / 2, p. 70-76 : ill <https://ieeexplore.ieee.org/abstract/document/1423822>

A framework for area-efficient concurrent online checkers design

Saltarelli, Pietro; Niazmand, Behrad; Hariharan, Ranganathan; Raik, Jaan; Jervan, Gert; Hollstein, Thomas MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 /

A framework for combining concurrent checking and online embedded test for low-latency fault detection in NoC routers
Saltarelli, Pietro; Niazmand, Behrad; Raik, Jaan; Govind, Vineeth; Hollstein, Thomas; Jervan, Gert; Hariharan, Ranganathan NOCS '15 : International Symposium on Networks-on-Chip : Vancouver, BC, Canada, September 28-30, 2015 2015 / [8] p. : ill <http://dx.doi.org/10.1145/2786572.2788713>

A framework for comprehensive automated evaluation of concurrent online checkers
Saltarelli, Pietro; Niazmand, Behrad; Raik, Jaan; Hariharan, Ranganathan; Jervan, Gert; Hollstein, Thomas Euromicro Conference on Digital System Design : DSD 2015 : 26-28 August 2015, Funchal, Madeira, Portugal : proceedings 2015 / p. 288-292 : ill <http://dx.doi.org/10.1109/DSD.2015.15>

From online fault detection to fault management in network-on-chips : a ground-up approach
Azad, Siavoosh Payandeh; Niazmand, Behrad; Janson, Karl; Nevin, George; Oyeniran, Adeboye Stephen; Putkaradze, Tsothe; Apneet Kaur; Raik, Jaan; Jervan, Gert; Ubar, Raimund-Johannes; Hollstein, Thomas Proceedings 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuit & Systems(DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 48-53 : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553>

From RTL liveness assertions to cost-effective hardware checkers
Hariharan, Ranganathan; Ghasempouri, Tara; Niazmand, Behrad; Raik, Jaan XXXIII Conference on Design of Circuits and Integrated Systems (DCIS) : proceedings 2018 / 6 p. : ill <https://doi.org/10.1109/DCIS.2018.8681487>

FSMD RTL design manipulation for clock interface abstraction
Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 10-13 August 2015, Kerala, India 2015 / p. 463-468 : ill <http://dx.doi.org/10.1109/ICACCI.2015.7275652>

Fully-fusible convolutional neural networks for end-to-end fused architecture with FPGA implementation
Dadras, Iman; Seydi, Sakineh; Ahmadilivani, Mohammad Hasan; Raik, Jaan; Salehi, Mostafa E. 2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2023 / 5 p. <https://doi.org/10.1109/ICECS58634.2023.10382831>

Functional self-test of high-performance pipe-lined signal processing architectures
Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart Microprocessors and microsystems 2015 / p. 909-918 : ill <https://doi.org/10.1016/j.micpro.2014.11.002> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Functional test generation for finite state machines
Ubar, Raimund-Johannes; Brik, Marina; Jutman, Artur; Raik, Jaan; Bengtsson, Tomas; Kumar, Shashi BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 205-208 : ill

GA-based test generation for sequential circuits
Brik, Marina; Raik, Jaan; Ubar, Raimund-Johannes; Ivask, Eero Proceedings of East-West Design & Test Workshop (EWDTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 30-34

Gate-level modelling of NBTI-induced delays under process variations
Copetti, Thiago; Cardoso Medeiros, Guilherme; Bolzani Poehls, Leticia; Vargas, Fabian; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 75-80 : ill <http://dx.doi.org/10.1109/LATW.2016.7483343>

Generating directed tests for C programs using RTL ATPG
Raik, Jaan; Drenkhan, Tiia; Jenihhin, Maksim; Viilukas, Taavi; Karputkin, Anton; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the IEEE 13th Workshop on RTL and High Level Testing (WRTL'12) 2012 / p. 1-6

Generic interconnect BIST for Network-on-Chip
Jutman, Artur; Ubar, Raimund-Johannes; Raik, Jaan DDECS : 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 13-16, 2005, Sopron, Hungary : proceedings 2005 / p. 224-227 : ill

A generic synthesizable NoC switch with a scalable testbench
Govind, Vineeth; Raik, Jaan; Ubar, Raimund-Johannes BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 91-94 : ill

Greedy alternative for the static compaction of sequential circuit test sequences
Raik, Jaan The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 133-136 : ill

Handbook of testing electronic systems

Novak, Ondrej; Gramatova, Elena; **Ubar, Raimund-Johannes; Jutman, Artur; Raik, Jaan** 2005
https://www.ester.ee/record=b2102523*est

Handling of SETs on NoC links by exploitation of inherent redundancy in circular input buffers [Online resource]

Janson, Karl; Pihlak, Rene; Azad, Siavoosh Payandeh; Niazmand, Behrad; Jervan, Gert; Raik, Jaan BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p.: ill <https://doi.org/10.1109/BEC.2018.8600989>

Hardware modeling for design verification and debug = Riistvara modelleerimine disaini verifitseerimise ja silumise jaoks

Tšepurov, Anton 2013 https://www.ester.ee/record=b2963501*est

Heterogeneous Approximation of DNN HW Accelerators based on Channels Vulnerability

Cherezova, Natalia; Pappalardo, Salvatore; Taheri, Mahdi; Ahmadiivani, Mohammad Hasan; Deveautour, Bastien; Bosio, Alberto; Raik, Jaan; Jenihhin, Maksim 2024 IFIP/IEEE 32nd International Conference on Very Large Scale Integration (VLSI-SoC) 2024 / 4 p. : ill <https://doi.org/10.1109/VLSI-SoC62099.2024.10767798>

Hierarchical analysis of short defects between metal lines in CMOS IC

Pleskacz, Witold A.; Jenihhin, Maksim; Raik, Jaan; Rakowski, Michal; Ubar, Raimund-Johannes; Kuzmicz, Wieslaw Proceedings : 11th EUROMICRO Conference on Digital System Design : Architectures, Methods and Tools : (DSD 2008) : September 3-5, 2008, Parma, Italy 2008 / p. 729-734 : ill <https://ieeexplore.ieee.org/document/4669309>

A hierarchical approach for devising area efficient concurrent online checkers

Niazmand, Behrad; Azad, Siavoosh Payandeh; Ghasempouri, Tara; Raik, Jaan; Jervan, Gert Proceedings 2nd IEEE International Test Conference in Asia : ITC-Asia 2018, 15-17 August 2018, Harbin, China 2018 / p. 139-144 : ill <https://doi.org/10.1109/ITC-Asia.2018.00034>

A hierarchical automatic test pattern generator based on using alternative graphs

Brik, Marina; Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 4th International Workshop Mixed Design of Integrated Circuits and Systems : MIXDES'97 : Poznan, Poland, 12-14 June 1997 1997 / p. 415-420

Hierarchical calculation of malicious faults for evaluating the fault-tolerance

Ubar, Raimund-Johannes; Devadze, Sergei; Jenihhin, Maksim; Raik, Jaan; Jervan, Gert; Ellervee, Peeter Proceedings : Fourth IEEE International Symposium on Electronic Design, Test and Applications : [DELTA 2008] : 23-25 January 2008, Hong Kong, SAR, China 2008 / p. 222-227 : ill <https://ieeexplore.ieee.org/document/4459544>

Hierarchical defect level test quality analysis

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; Raik, Jaan; Ubar, Raimund-Johannes VILAB User Forum 2000 / [11] p

Hierarchical defect-oriented fault simulation for digital circuits

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; Raik, Jaan; Ubar, Raimund-Johannes IEEE European Test Workshop : 23-26 May 2000, Cascais, Portugal : ETW 2000 : proceedings 2000 / p. 69-74 : ill <https://ieeexplore.ieee.org/document/873781>

Hierarchical defect-oriented fault simulation for digital circuits

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; Raik, Jaan; Ubar, Raimund-Johannes IEEE European Test Workshop 2000 / p. 151-156 <https://ieeexplore.ieee.org/document/873781>

Hierarchical fault simulation for finite state machines

Brik, Marina; Raik, Jaan; Ubar, Raimund-Johannes The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 145-148 : ill

Hierarchical fault simulation in digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina International Symposium on Signals, Circuits and Systems : SCS 2001 : July 10-11, 2001, Iasi, Romania : proceedings 2001 / p. 181-184 : ill

Hierarchical identification of NBTI-critical gates in nanoscale logic

Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Hierarchical identification of untestable faults in sequential circuits

Raik, Jaan; Ubar, Raimund-Johannes; Krivenko, Anna; Kruus, Margus 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 668-671 : ill <http://dx.doi.org/10.1109/DSD.2007.4341539>

Hierarchical physical defect reasoning in digital circuits

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan; Brik, Marina Estonian journal of engineering 2011 / 3, p. 185-200

Hierarchical test generation for combinational circuits with real defects coverage

Cibakova, Tatiana; Fischerova, Maria; Gramatova, Elena; Kuzmich, W.; Pleskacz, Witold A.; Raik, Jaan; Ubar, Raimund-Johannes Microelectronics reliability 2002 / p. 1141-1149 : ill <https://www.sciencedirect.com/science/article/pii/S002627140200080X>

Hierarchical test generation for complex digital systems with control and data processing parts

Ubar, Raimund-Johannes; Raik, Jaan "Test, Assembly and Packaging" : SEMICON Technical Symposium : Singapur, May 3-6, 1999 1999 / p. 43-52

Hierarchical test generation for digital circuits represented by Decision Diagrams : thesis on informatics and system engineering

Raik, Jaan 2001 https://www.ester.ee/record=b1578107*est

Hierarchical test generation for digital systems

Brik, Marina; Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Mixed design of integrated circuits and systems 1998 / p. 131-136: ill https://link.springer.com/chapter/10.1007/978-1-4615-5651-0_20

Hierarchical test generation for digital systems based on combining bottom-up and top-down approaches

Raik, Jaan; Ubar, Raimund-Johannes World Multiconference on Systemics, Cybernetics and Informatics, July 12-16, 1998, Orlando, Florida : proceedings. Vol. 1 1998 / p. 374-381: ill

Hierarchical test generation with multi-level decision diagram models

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 7th IEEE North Atlantic Test Workshop, West Greenwich RI, USA, May 28-29, 1998 1998 / p. 26-33
https://www.academia.edu/67811738/Hierarchical_Test_Generation_with_Multi_Level_Decision_Diagram_Models?hb-g-sw=7883185

Hierarchical test generation. SEMI show slides

Ubar, Raimund-Johannes; Raik, Jaan "Test, Assembly and Packaging" : SEMICON Technical Symposium : Singapur, May 3-6, 1999 1999 / p. 53-64

Hierarchical test pattern generation and untestability identification techniques for synchronous sequential circuits = Hierarhilised testintegreerimise ja mittetestitavuse identifitseerimise meetodid sünkroonsetele järjestikskeemidele

Rannaste, Anna 2010 https://www.ester.ee/record=b2637391*est

Hierarchical timing-critical paths analysis in sequential circuits

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan; Devadze, Sergei; Kostin, Sergei 2018 IEEE 28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS 2018) : 2 – 4 July 2018, Spain 2018 / 6 p. : ill <https://doi.org/10.1109/PATMOS.2018.8464176>

High level fault modeling in digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Brik, Marina; Raik, Jaan Synergies between Information and Automation : 49. Internationales Wissenschaftliches Kolloquium, 27.-30.9.2004, Technische Universität Ilmenau, Germany. Volume 2 2004 / p. 486-491

High quality test generation for digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Kruus, Helena; Raik, Jaan Romanian journal of information science and technology 2005 / 1, p. 73-84 : ill

High-Level Combined Deterministic and Pseudo-exhaustive Test Generation for RISC Processors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan 2019 IEEE European Test Symposium (ETS) : ETS 2019, May 27-31, 2019, Baden-Baden, Germany : Proceedings 2019 / 6 p. : ill <https://doi.org/10.1109/ETS.2019.8791526>

High-level combined deterministic and pseudo-exhaustive test generation for RISC processors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Gürsoy, Cemil Cem; Raik, Jaan 2019 IEEE European Test Symposium (ETS) : proceedings 2019 / 6 p. : ill <https://doi.org/10.1109/ETS.2019.8791526>

High-level decision diagram based fault models for targeting FSMs

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 353-358 : ill <http://dx.doi.org/10.1109/DSD.2006.60>

High-Level Decision Diagram manipulations for code coverage analysis

Minakova, Karina; Reinsalu, Uljana; Tšepurov, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level decision diagram simulation for diagnosis and soft-error analysis

Raik, Jaan; Repinski, Urmaz; Jenihhin, Maksim; Chepurov, Anton Design and test technology for dependable systems-on-chip 2011 / p. 294-309 : ill <https://www.igi-global.com/chapter/high-level-decision-diagram-simulation/51406>

High-level decision diagrams based coverage metrics for verification and test

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes LATW 2009 : 10th IEEE Latin American Test Workshop : Buzios, Rio de Janeiro, Brazil, March 2-5, 2009 2009 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2009.4813792>

High-level decision diagrams for improving simulation performance of digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Morawiec, Adam SCI 2000 : World Multiconference on Systemics, Cybernetics and Informatics : July 23-26, 2000, Orlando, Florida, USA : proceedings. Volume IX, Industrial Systems 2000 / p. 62-67 : ill <https://hal.science/hal-01396447v1>

High-level design error diagnosis using backtrace on decision diagrams

Raik, Jaan; Repinski, Urmaz; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton 28th Norchip Conference : Tampere, Finland, 15-16 November 2010 : conference program and papers 2010 / [4] p. : ill <http://dx.doi.org/10.1109/NORCHIP.2010.5669486>

High-level fault diagnosis in RISC processors with Implementation-Independent Functional Test

Oyeniran, Adeboye Stephen; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) : Nicosia, Cyprus : 04-06 July 2022 2022 / p. 32-37 <https://doi.org/10.1109/ISVLSI54635.2022.00019>

High-Level Implementation-Independent Functional Software-Based Self-Test for RISC Processors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Journal of electronic testing : theory and applications 2020 / p. 87-103 <https://doi.org/10.1007/s10836-020-05856-7>

High-level intellectual property obfuscation via decoy constants

Aksoy, Levent; Nguyen, Quang-Linh; Almeida, Felipe; Raik, Jaan; Flottes, Marie-Lise; Dupuis, Sophie; Pagliarini, Samuel Nascimento 2021 IEEE 27th International Symposium on On-Line Testing and Robust System Design (IOLTS) : Torino, Italy, 28-30 June 2021 2021 / p. 1-7 <https://doi.org/10.1109/IOLTS52814.2021.9486714>

High-level path activation technique to speed up sequential circuit test generation

Raik, Jaan; Ubar, Raimund-Johannes European Test Workshop 1999 : proceedings, May 25-28, 1999, Constance, Germany 1999 / p. 84-89 : ill <https://ieeexplore.ieee.org/document/804289>

High-level synthesis and test in the MOSCITO-based virtual laboratory

Schneider, Andre; Diener, Karl-Heinz; Jervan, Gert; Peng, Z.; Raik, Jaan; Ubar, Raimund-Johannes; Hollstein, Thomas; Glesner, M. BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 287-290 : ill

High-level test generation for processing elements in many-core systems

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Azad, Siavoosh Payandeh; Raik, Jaan 12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC2017), July 12-14, 2017, Madrid, Spain : proceedings 2017 / 8 p. : ill <http://dx.doi.org/10.1109/ReCoSoC.2017.8016156>

High-level test synthesis with hierarchical test generation

Jervan, Gert; Eles, Petru; Peng, Zebo; Raik, Jaan; Ubar, Raimund-Johannes 17th NORCHIP Conference : Oslo, Norway, 8-9 November 1999 : proceedings 1999 / p. 291-296

Holistic approach for Fault-Tolerant Network-on-Chip based many-core systems [Online resource]

Azad, Siavoosh Payandeh; Niazmand, Behrad; Raik, Jaan; Jervan, Gert; Hollstein, Thomas arXiv.org 2016 / [8] p. : ill

How to generate high quality tests for digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Kruus, Helena; Raik, Jaan 2004 International Semiconductor Conference : 27th edition, October 4-6, 2004, Sinaia, Romania : CAS 2004 proceedings. Volume 2 2004 / p. 459-462 : ill <http://dx.doi.org/10.1109/SMICND.2004.1403048>

How to prove that a circuit is fault-free?

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan Proceedings : 15th Euromicro Conference on Digital System Design DSD 2012 : 5-8 September 2012, Cesme, Izmir, Turkey 2012 / p. 427-430 : ill https://www.researchgate.net/publication/262271409_How_to_Prove_that_a_Circuit_is_Fault-Free

"Hullkoer" käis Tehnikaülikoolis : [TTÜs pidas loengu Linux International'i direktor John "Maddog" Hall]

Kruus, Margus; Raik, Jaan Mente et Manu 2002 / lk. 3 : fot https://www.ester.ee/record=b1242496*est

"Hullkoer" käis Tehnikaülikoolis : [TTÜs pidas loengu Linux International'i direktor John "Maddog" Hall]
Kruus, Margus; Raik, Jaan Arvutikasutaja 2002 / lk. 5 : fot

Hybrid protection of digital FIR filters

Aksoy, Levent; Nguyen, Quang-Linh; **Almeida, Felipe; Raik, Jaan;** Flottes, Marie-Lise; Dupuis, Sophie; **Pagliarini, Samuel Nascimento** IEEE transactions on Very Large Scale Integration (VLSI) Systems 2023 / p. 812-825 : ill
<https://doi.org/10.1109/TVLSI.2023.3253641> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

HyFBIST : hybrid functional built-in self-test in microprogrammed data-paths of digital systems

Ubar, Raimund-Johannes; Mazurova, Natalja; Smahitina, Julia; **Orasson, Elmet; Raik, Jaan** Proceedings of the 11th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2004 : Szczecin, Poland, 24-26 June 2004 2004 / p. 497-502 : ill

Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits

Jenihhin, Maksim; Squillero, Giovanni; **Tihomirov, Valentin; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill <https://doi.org/10.1007/s10836-016-5589-x> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Identifying NBTI-critical paths in nanoscale logic

Ubar, Raimund-Johannes; Vargas, Fabian; **Jenihhin, Maksim; Raik, Jaan; Kostin, Sergei;** Bolzani Poehls, Leticia 16th Euromicro Conference series on Digital System Design : DSD 2013 : proceedings : 4-6 September 2013, Santander, Spain 2013 / p. 136-141 : ill

Identifying untestable faults in sequential circuits using test path constraints

Viilukas, Taavi; Karputkin, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill <https://link.springer.com/article/10.1007/s10836-012-5312-5>

IEEE Euroopa 10. Testisümposion Tallinnas : [21.-26. maini 2005 hotellis "Olümpia" ja konverentsi õppeseminarid TTÜ Energeetikamajas]

Raik, Jaan Mente et Manu 2006 / 18. jaan., lk. 5 https://www.ester.ee/record=b1242496*est

IEEE European Test Symposium (ETS)

Eggersgluss, Stephan; Hamdioui, Said; **Jutman, Artur;** Michael, Maria K.; **Raik, Jaan** 2019 IEEE International Test Conference (ITC) 2019 / 4 p <https://doi.org/10.1109/ITC44170.2019.9000148> [Conference proceeding at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

IMMizer : an innovative cost-effective method for minimizing assertion sets

Heidari Iman, Mohammad Reza; Raik, Jaan; Jervan, Gert; Ghasempouri, Tara 2022 25th Euromicro Conference on Digital System Design (DSD) : Maspalomas, Spain 2022 : proceedings 2022 / p. 671 - 678 <https://doi.org/10.1109/DSD57027.2022.00095>
[Article at Scopus](#) [Article at WOS](#)

Implementation-independent functional test for transition delay faults in microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / p. 646-650 <https://doi.org/10.1109/DSD51259.2020.00105>

Implementation-independent functional test generation for RISC microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan VLSI-SoC 2019 : 27th IFIP/IEEE International Conference on Very Large Scale Integration : [proceedings] 2019 / p. 82-87 : ill <https://doi.org/10.1109/VLSI-SoC.2019.8920323>

Implementation-independent test generation for a large class of faults in RISC processor modules

Jenihhin, Maksim; Oyeniran, Adeboye Stephen; Raik, Jaan; Ubar, Raimund-Johannes 24th Euromicro Conference on Digital System Design (DSD) 2021 <https://doi.org/10.1109/DSD53832.2021.00090>

Improved fault emulation for synchronous sequential circuits

Raik, Jaan; Ellervee, Peeter; Tihomirov, Valentin; Ubar, Raimund-Johannes Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 72-78 : ill

Integrated modelling, fault management, verification and reliable design environment for cyber-physical systems

Raik, Jaan; Rauwerda, Gerard; Zhao, Yong; **Shibin, Konstantin** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 74

Integration of digital test tools to the internet-based environment MOSCITO

Schneider, Andre; Diener, Karl-Heinz; Elst, Günter; **Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes** SCI 2003 : the 7th World Multiconference on Systemics, Cybernetics and Informatics : July 27-30, 2003, Orlando, Florida, USA : proceedings. Volume VIII, Applications of Informatics and Cybernetics in Science and Engineering 2003 / p. 136-141 : ill

Interactive presentation abstract : automated correction of design errors by edge redirection on high-level decision diagrams [Electronic resource]

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan IEEE International High Level Design Validation and Test Workshop (HLDVT'11), November 9-11, 2011, Napa Valley, CA 2011 / p. 83 : ill. [CD-ROM]
<http://doi.ieeecomputersociety.org/10.1109/HLDVT.2011.6113980>

Internet based test generation and fault simulation

Ivask, Eero; Ubar, Raimund-Johannes; Raik, Jaan; Schneider, Andre IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Győr, Hungary, April 18-20, 2001 2001 / p. 57-60 : ill

Internet-based collaborative test generation with MOSCITO [Electronic resource]

Schneider, Andre; **Ivask, Eero;** Miklos, P.; **Raik, Jaan;** Diener, Karl-Heinz; **Ubar, Raimund-Johannes;** Cibakova, Tatiana; Gramatova, Elena SIGDA publications on CD-ROM : DATE'02 : Design, Automation and Test in Europe, Paris, France, March 4-8, 2002 2002 / [6] p. [CD-ROM] https://www.cecs.uci.edu/~papers/date07/PAPERS/2002/DATE02/PDFFILES/02E_2.PDF

Internet-based software for teaching test of digital circuits

Ubar, Raimund-Johannes; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Evartson, Teet; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 4th European Workshop on Microelectronics Education : EWME 2002, Spain, May 23-24, 2002 2002 / p. 317-320 : ill <https://ieeexplore.ieee.org/document/1003344>

Internet-based testability-driven test generation in the virtual environment MOSCITO

Schneider, Andre; Diener, Karl-Heinz; Elst, G.; **Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes** International Federation for Information Processing IFIP : International Workshop on IP-Based SoC Design 2002 : proceedings : Grenoble, October 30-31, 2002 2002 / p. 357-362 : ill <http://publica.fraunhofer.de/dokumente/N-287433.html>

Investigations of the diagnosability of digital networks with BIST

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan 10th IEEE Latin American Test Workshop : 2-5 March 2009, Brazil 2009 / [6] p. : ill

Jaan Raik : müütidest Eesti elektroonikatööstuse väljavaadete ümber

Raik, Jaan err.ee 2022 [Jaan Raik: müütidest Eesti elektroonikatööstuse väljavaadete ümber](#)

Jaan Raik : Nurkse juhtumist ilma paranoiata [Võrguväljaanne]

Raik, Jaan err.ee 2019 / fot [Jaan Raik: Nurkse juhtumist ilma paranoiata](#)

Jaan Raik : valedega "korruptsiooni" vastu [Võrguväljaanne]

Raik, Jaan err.ee 2020 / fot [Jaan Raik: valedega "korruptsiooni" vastu](#) vaata ka: [Keegan McBride: vastukaja artiklile "Valedega "korruptsiooni" vastu" \(err.ee 24.01.2020\)](#)

Jaan Raik: Computers must undergo a revolution in order to continue their rapid development

Raik, Jaan Estonian Centre of Excellence in ICT Research 2021 / p. 43-47 : ill <http://www.digar.ee/id/nlib-digar:634779>
https://www.ester.ee/record=b5456158*est

Jaan Raik: kiibidisain aitaks saada Eestil jõukaks tehnoloogiamaaks

Maidla, Margus novaator.err.ee 2023

Kakskümmend aastat hiljem : [vestlus arvutisüsteemide dignostika ja verifitseerimise õppetooli professori Jaan Raikiga]

Raik, Jaan Mente et Manu 2013 / lk. 10-12 : fot https://www.ester.ee/record=b1242496*est

Keynote: cost-efficient reliability for Edge-AI chips

Jenihhin, Maksim; Taheri, Mahdi; Cherezova, Natalia; Ahmadilivani, Mohammad Hasan; Selg, Hardi; Jutman, Artur; Shibin, Konstantin; Tsertov, Anton; Devadze, Sergei; Kodamanchili, Rama Mounika; Rafiq, Ahsan; Raik, Jaan; Daneshtalab, Masoud 2024 IEEE 25th Latin American Test Symposium (LATS) 2024 / 2 p <https://doi.org/10.1109/LATS62223.2024.10534610> [Article at Scopus](#)

Kiibikeskus kui ellujäämisvõimalus

Vaaks, Eveliis Trialoog 2025 <https://trialoog.taltech.ee/kiibikeskus-kui-ellujamisvoimalus/>

Kiibikriis: kas maailmalõpp või Eesti võimalus?

Raik, Jaan Postimees 2022 / Lk. 12 <https://dea.digar.ee/article/postimees/2021/12/14/12.4>

Kuidas teemant tehnikaülikooli tuli

Raik, Jaan Tallinna Tehnikaülikooli aastaraamat 2009 2010 / lk. 40-43 : ill https://www.ester.ee/record=b1212786*est

Kuidas testida arvutivõrku ränikiibil

Raik, Jaan; Govind, Vineeth A & A 2010 / 4, lk. 35-37 https://artiklid.elnet.ee/record=b2286479*est

Layout to logic defect analysis for hierarchical test generation

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Pleskacz, Witold A.; Rakowski, Michal Proceedings of the 2007 IEEE Workshop on Design and Diagnostic Circuits and Systems : April 11-13, 2007, Krakow, Poland 2007 / p. 35-40 : ill <http://dx.doi.org/10.1109/DDECS.2007.4295251>

LiD-CAT: A lightweight detector for cache ATtacks

Reinbrecht, Cezar; Hamdioui, Said; Taouil, Mottaqiallah; **Niazmand, Behrad; Ghasempouri, Tara; Raik, Jaan;** Sepulveda, Johanna 2020 IEEE European Test Symposium (ETS) : ETS 2020, May 25-29, 2020 Tallinn, Estonia : proceedings 2020 / 6 p. : ill <https://doi.org/10.1109/ETS48528.2020.9131603>

Linear algorithms for recognizing and parsing superpositional graphs

Peder, Ahti; Nestra, Härmel; **Raik, Jaan; Tombak, Mati; Ubar, Raimund-Johannes** Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 325-339 : ill <http://dx.doi.org/10.2298/FUEE1103325P>

Linear algorithms for testing superpositional graphs

Peder, Ahti; Nestra, Härmel; **Raik, Jaan; Tombak, Mati; Ubar, Raimund-Johannes** Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 111-118 : ill

Localization of bugs in processor designs using zamiaCAD framework

Tšepurov, Anton; Tihhomirov, Valentin; Jenihhin, Maksim; Raik, Jaan 13th International Workshop on Microprocessor Test and Verification (MTV 2012) Common Challenges and Solutions : Austin, USA, December 10–12, 2012 2012 / p. 1-6 <https://ieeexplore.ieee.org/document/6519733>

Logic simulation and fault collapsing with shared structurally synthesized BDDs

Mironov, Dmitri; Ubar, Raimund-Johannes; Raik, Jaan 2014 19th IEEE European Test Symposium (ETS) : May 26th-30th, 2014, Paderborn, Germany : proceedings 2014 / [2] p. : ill

Logic-based implementation of fault-tolerant routing in 3D Network-on-Chips

Niazmand, Behrad; Azad, Siavoosh Payandeh; Flich, Jose; **Raik, Jaan; Jervan, Gert; Hollstein, Thomas** 2016 Tenth IEEE/ACM International Symposium on Networks-on-Chip (NOCS) : Nara, Japan, 31 August - 2 September 2016 2016 / [8] p. : ill <https://doi.org/10.1109/NOCS.2016.7579317>

Low-area boundary BIST architecture for mesh-like network-on-chip

Raik, Jaan; Govind, Vineeth Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia 2012 / p. 95-100 : ill

Low-cost CAD software for teaching digital test

Ubar, Raimund-Johannes; Raik, Jaan; Paomets, Priidu First European Workshop on Microelectronics Education, Villard de Lans, France, February 5-6, 1996 : proceedings 1996 / p. 48

Low-cost CAD system for teaching digital test

Ubar, Raimund-Johannes; Raik, Jaan; Paomets, Priidu; Ivask, Eero; Jervan, Gert; Markus, Antti Microelectronics education : proceedings of the European Workshop, Grenoble, France, 5-6 Feb 1996 1996 / p. 185-188

Machine vision for automated collaborative robot programming in manufacturing industrial factories

Ahmadilivani, Mohammad Hasan; Karatopuk, Emre; Roots, Marten; Raik, Jaan Smart machines and systems at the service of mankind : Abstracts of the 12th annual entrepreneurship and innovation conference 2024 / p. 10 <https://conference.euas.eu/2024/wp-content/uploads/2024/10/ConferenceProceedings2024-1.pdf> https://www.ester.ee/record=b5705417*est

Macro level defect-oriented diagnosability of digital circuits

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 53-56 : ill

Macro level defect-oriented diagnosability of digital circuits

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 149-152 : ill

Measuring and identifying aging-critical paths in FPGAs

Pfeifer, Petr; **Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes;** Pliva, Zdenek MEDIAN 2015 : the 4th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : March 13, 2015, Grenoble, France 2015 / p. 56-61 : ill

A methodology for automated mining of compact and accurate assertion sets

Heidari Iman, Mohammad Reza; Raik, Jaan; Jenihhin, Maksim; Jervan, Gert; Ghasempouri, Tara 2021 IEEE Nordic Circuits and Systems Conference (NorCAS) : Oslo, Norway, October 26-27 2021 / 7 p. : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9599865> <https://doi.org/10.1109/NorCAS53631.2021.9599865>

Methods for improving the accuracy and efficiency of fault simulation in digital systems = Meetodid digitaalsüsteemide rikete simuleerimise täpsuse ja efektiivsuse tõstmiseks

Kõusaar, Jaak 2019 <https://digi.lib.ttu.ee/i/?11667>

Mikk Raud: Eestil on aeg oma kiibipotentsiaal ellu äratada

Arjakas, Merili diplomaatia.ee 2023

Mikroelektroonika kiipide testimise tarkvara turbo-tester : kommentaar Eesti Teaduste Akadeemia Bernhard Schmidti preemia pälvinud tööle

Raik, Jaan Tallinna Tehnikaülikooli aastaraamat 2007 2008 / lk. 275-278

Mixed hierarchical-functional fault models for targeting sequential cores

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Jenihhin, Maksim Journal of systems architecture 2008 / 3/4, p. 465-477 : ill <https://www.sciencedirect.com/science/article/abs/pii/S1383762107001166>

Mixed-level defect simulation in data-paths of digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 617-620 : ill <https://ieeexplore.ieee.org/document/1003333>

Mixed-level deterministic-random test generation for digital systems

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 335-340

Mixed-level identification of fault redundancy in microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Gürsoy, Cemil Cem; Raik, Jaan LATS 2019 : 20th IEEE Latin American Test Symposium : Santiago, Chile, March 11th - 13th 2019 2019 / 6 p. : ill <https://doi.org/10.1109/LATW.2019.8704591>

Mixed-level test generator for digital systems

Brik, Marina; Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 1997 / 4, p. 271-282 : ill

ML-based online design error localization for RISC-V implementations

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter; Raik, Jaan 2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS) : IOLTS 2023 : July 3rd-5th, 2023, Platani, Chania (Crete), Greece : proceedings 2023 / 7 p. <https://doi.org/10.1109/IOLTS59296.2023.10224864>

Modeling and experimental analysis of the mass loading effect on micro-ionic polymer actuators using step response identification

Dadras, Iman; Ghenna, Sofiane; Grondel, Sébastien; Cattani, Éric; Raik, Jaan; Aabloo, Alvo; Banerji, Saoni Journal of Microelectromechanical Systems 2021 / p. 243-252 : ill <https://doi.org/10.1109/JMEMS.2021.3060897> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Modeling and simulation of circuits with shared structurally synthesized BDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; Raik, Jaan; Viies, Vladimir Microprocessors and microsystems 2017 / p. 56-61 : ill <https://doi.org/10.1016/j.micpro.2016.09.006> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Modeling for multi-view interference analysis of design aspects in MPSoC designs

Vain, Jüri; Apneet Kaur; Tsiopoulos, Leonidas; Raik, Jaan; Jenihhin, Maksim RESCUE 2017 : Workshop on Reliability, Security and Quality : ETS17 Fringe Workshop, May 25-26, 2017, Limassol, Cyprus 2017 / p. 1-6 <http://www.ets17.org.cy/workshop/rescue-workshop.html>

Modeling microprocessor faults on high-level decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Istenberg, Martin; Wuttke, Heinz-Dietrich DSN 2008 : supplemental : 2008 IEEE International Conference on Dependable Systems & Networks With FTCS & DCC (DSN) : June 24-27, 2008, Anchorage, Alaska 2008 / p. C17-C22 : ill. [CD-ROM] [https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08\(LAAS\)_files/Slides/WDSN08S-04-Ubar.pdf](https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08(LAAS)_files/Slides/WDSN08S-04-Ubar.pdf)

Module level defect simulation in digital circuits

Kuzmich, Wieslaw; Pleskacz, Witold A.; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 2001 / 4, p. 253-268

Multi-fragment Markov model guided online test generation for MPSoC

Vain, Jüri; Tsiopoulos, Leonidas; Kharchenko, Vyacheslav; Apneet Kaur; Jenihhin, Maksim; Raik, Jaan ICTERI 2017 : ICT in Education, Research and Industrial Applications. Integration, Harmonization and Knowledge Transfer : proceedings of the 13th International Conference on ICT in Education, Research and Industrial Applications. Integration, Harmonization and Knowledge Transfer, Kyiv, Ukraine, May 15-18, 2017 / p. 594-607 : ill <http://www.scopus.com/inward/record.uri?eid=2-s2.0-85020540459&partnerID=40&md5=af226e25c344c52689f23bf5c39cc267> <http://ceur-ws.org/Vol-1844/10000594.pdf> [Conference proceedings at Scopus](#) [Article at Scopus](#)

Multi-level fault simulation of digital systems on decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina The First IEEE International Workshop on Electronic Design, Test and Applications : DELTA 2002, 29-31 January 2002, Christchurch, New Zealand : proceedings 2002 / p. 86-91 : ill

Multiple fault diagnosis with BDD based Boolean differential equations

Ubar, Raimund-Johannes; Raik, Jaan; Kostin, Sergei; Kõusaar, Jaak BEC 2012 : 2012 13th Biennial Baltic Electronics Conference : proceedings of the 13th Biennial Baltic Electronics Conference : October 3-5, 2012, Tallinn, Estonia 2012 / p. 77-80 : ill

Multiple stuck-at-fault detection theorem

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia 2012 / p. 236-241 : ill

Multiple-objective backtrace for solving test generation constraints

Mekler, A.; Raik, Jaan International Symposium on System-on-Chip : November 19-21, 2003, Tampere, Finland : proceedings 2003 / p. 123-126 : ill <https://ieeexplore.ieee.org/document/1267732>

Multi-valued simulation with binary decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan Proceedings IEEE European Test Workshop, Cagliari, Italy, May 28-30, 1997 / p. 28-29

Multi-view modeling for MPSoC design aspects [Online resource]

Vain, Jüri; Apneet Kaur; Tsiopoulos, Leonidas; Raik, Jaan; Jenihhin, Maksim BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 / 4 p.: ill <https://doi.org/10.1109/BEC.2018.8600986>

Mutation analysis for systemC designs at TLM

Guarnieri, Valerio; Bombieri, Nicola; Pravadelli, Graziano; Fummi, Franco; Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes 12th IEEE Latin American Test Workshop (LATW) : Porto de Galinhas, Brasil, 27-30 March 2011 / [6] p <https://ieeexplore.ieee.org/document/5985925>

Mutation analysis with high-level decision diagrams

Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Tšepurov, Anton; Ubar, Raimund-Johannes; Guglielmo, Giuseppe di; Fummi, Franco LATW2010 : 11th Latin-American TestWorkshop, March 28-31, 2010, Punta del Este, Uruguay 2010 / [6] p. [CD-ROM] <https://ieeexplore.ieee.org/document/5550336>

Mutation-based verification and error correction in high-level designs = Mutatsioonidel põhinev verifitseerimine ja vigade parandamine kõrgtaseme skeemides

Hantson, Hanno 2015 https://www.ester.ee/record=b4518212*est

Nanoelectronics aging mitigation using SSBDD based techniques and dedicated sensors

Ubar, Raimund-Johannes; Vargas, Fabian; Jenihhin, Maksim; Raik, Jaan MEDIAN Workshop on Circuit Reliability : Modeling and Monitoring, Rome, Italy, February 25, 2013 / [1] p

Negative correlation between functional connectivity and small-worldness in the alpha frequency band of a healthy brain

Päeske, Laura; Hinrikus, Hiie; Lass, Jaanus; Raik, Jaan; Bachmann, Maie Frontiers in Physiology 2020 / Art. nr. 910 <https://doi.org/10.3389/fphys.2020.00910> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

New built-in self-test scheme for SoC interconnect

Jutman, Artur; Ubar, Raimund-Johannes; Raik, Jaan The 9th World Multi-Conference on Systemics, Cybernetics and Informatics : WMSCI 2005 : July 10-13, 2005, Orlando, Florida, USA. Vol. IV 2005 / p. 19-24 : ill https://www.researchgate.net/publication/237375234_New_Built-In_Self-Test_Scheme_for_SoC_Interconnect

New categories of Safe Faults in a processor-based Embedded System

Gürsoy, Cemil Cem; Jenihhin, Maksim; Oyeniran, Adeboye Stephen; Piumatti, Davide; Raik, Jaan; Sonza Reorda, Matteo; Ubar, Raimund-Johannes 2019 22nd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Cluj-Napoca, Romania : proceedings 2019 / 4 p. : ill <https://doi.org/10.1109/DDECS.2019.8724642>

New fault models and self-test generation for microprocessors using High-Level Decision Diagrams

Jasnetski, Artjom; **Raik, Jaan; Tšertov, Anton; Ubar, Raimund-Johannes** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 251-254 : ill

New method of testability calculation to guide RT-level test generation

Raik, Jaan; Nõmmeots, Tanel; Ubar, Raimund-Johannes 4th IEEE Latin-American Test Workshop : LATW2003 : Natal, Brazil, February 16-19, 2003 2003 / p. 46-51 : ill <https://link.springer.com/article/10.1007/s10836-005-5288-5>

New technique for hierarchical identification of untestable faults in sequential circuits

Krivenko, Anna; Ubar, Raimund-Johannes; Raik, Jaan; Kruus, Margus Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / lk. 155-158 : ill

Noore teadlase preemia on ihaldusväärne : [Vabariigi Presidendi kultuurirahastu noore teadlase preemia sai Jaan Raik : Jaan Raigi kommentaaridega]

Lill, Anne; **Raik, Jaan** Linnaleht 2004 / lk. 4 : fot

Novel architectures for contractive autoencoders with embedded learning

Kerner, Madis; Tammemäe, Kalle; Raik, Jaan; Hollstein, Thomas 2020 17th Biennial Baltic electronics conference, Tallinn, Estonia, October 6-8, 2020 : proceedings 2020 / 6 p. : ill <https://doi.org/10.1109/BEC49624.2020.9277246>

Novel Neural Network accelerator architectures for FPGAs = Uudsed närvivõrkude kiirendite arhitektuurid FPGAdele

Kerner, Madis 2024 https://www.ester.ee/record=b5675484*est <https://digikogu.taltech.ee/et/Item/3568fe35-19c3-43e6-9525-73c79371ab13> <https://doi.org/10.23658/taltech.16/2024>

A novel random approach to diagnostic test generation

Osimiry, Emmanuel Ovie; Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan 2nd IEEE NORCAS Conference : 1-2 November 2016, Copenhagen, Denmark 2016 / [4] p. : ill <https://doi.org/10.1109/NORCHIP.2016.7792915>

NV-SP: A new high performance and low energy NVM-Based scratch pad

Shalabi, Ameer; Paul, Kolin; Ghasempouri, Tara; Raik, Jaan 2020 IEEE Computer Society Annual Symposium on VLSI : ISVLSI 2020, 6-8 July 2020, Limassol, Cyprus 2020 / art. 19876866, p. 54-59 <https://doi.org/10.1109/ISVLSI49217.2020.00020>

Nädala lood: jätkuvad halvad uudised ehitusest

Rõuk, Viivika aripaev.ee 2023 [Nädala lood: jätkuvad halvad uudised ehitusest](#)

On efficient logic-level simulation of digital circuits represented by the SSBDD model

Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 621-624 : ill <https://ieeexplore.ieee.org/document/1003334>

On reusability of verification assertions for testing

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Tšepurov, Anton BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 151-154 : ill

On reusability of verification assertions for testing

Jenihhin, Maksim; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 43-46 : ill

On test generation for microprocessors for extended class of functional faults

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan VLSI-SoC: New technology enabler : 27th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2019 Cusco, Peru, October 6-9, 2019 : Revised and Extended Selected Papers 2020 / p. 21-44 https://doi.org/10.1007/978-3-030-53273-4_Conference_proceedings_at_Scopus_Article_at_Scopus

On the combined use of HLDDs and EFSMs for functional ATPG

Di Guglielmo, Giuseppe; Fummi, Franco; **Jenihhin, Maksim; Pravadelli, Graziano; Raik, Jaan; Ubar, Raimund-Johannes** 5th IEEE East-West Design & Test Symposium EWDTS 2007 : September 7-10, 2007, Yerevan, Armenia 2007 / p. 503-508 : ill

On the reuse of TLM mutation analysis at RTL

Guarnieri, Valerio; **Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2012 / p. 435-448 : ill <https://link.springer.com/article/10.1007/s10836-012-5303-6>

On using genetic algorithm for test generation

Brik, Marina; Raik, Jaan; Ubar, Raimund-Johannes; Ivask, Eero BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 233-236 : ill

Open-source framework and practical considerations for translating RTL VHDL to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan IP-SoC 2012 : IP Embedded System Conference & Exhibition : Grenoble, France, Dec. 4-5, 2012 2012 <https://www.design-reuse.com/articles/32685/translating-rtl-vhdl-to-systemc.html>

Optimization methodologies for Cycle-Accurate SystemC models converted from RTL VHDL

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan IP-SoC 2013 : IP embedded system conference and exhibition : Grenoble, France, November 6-7, 2013 2013

Optimization of structurally synthesized BDDs

Ubar, Raimund-Johannes; Vassiljeva, T.; Raik, Jaan; Jutman, Artur; Tombak, Mati; Peder, Ahti Proceedings of the Fourth IASTED International Conference on Modelling, Simulation, and Optimization : August 17-19, 2004, Kawai, Hawaii, USA 2004 / p. 234-240 : ill https://www.academia.edu/22101496/Optimization_of_structurally_synthesized_BDDs

Parallel critical path tracing fault simulation in sequential circuits

Kõusaar, Jaak; Ubar, Raimund-Johannes; Kostin, Sergei; Devadze, Sergei; Raik, Jaan Proceedings of 25th International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS : MIXDES 2018 : Gdynia, Poland, June 21–23, 2018 2018 / p. 305-310 : ill <https://doi.org/10.23919/MIXDES.2018.8436880>

Parallel exact critical path tracing fault simulation with reduced memory requirements

Devadze, Sergei; Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur 4th International Conference on Design and Technology of Integrated Systems in Nanoscale Era : DTIS'09 : Cairo, Egypt, April 6-9, 2009 2009 / p. 155-160 : ill <https://ieeexplore.ieee.org/document/4938046>

Parallel fault backtracing for calculation of fault coverage

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur Proceedings of the ASP-DAC 2008 : [13th] Asia and South Pacific Design Automation Conference 2008 : January 21-24, 2008, COEX, Seoul, Korea 2008 / p. 667-672 : ill https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel fault backtracing for calculation of fault coverage

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur 43rd International Conference on Microelectronics, Devices and Materials and the Workshop on Electronic Testing : September 12. - September 14.2007, Bled, Slovenia : MIDEM conference 2007 proceedings 2007 / p. 165-170 : ill https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel fault simulation in digital circuits

Aarna, Margit; Raik, Jaan; Ubar, Raimund-Johannes Proc. of 42nd International Scientific Conference of Riga Technical University 2001 / p. 91-94

Parallel fault simulation in digital circuits

Aarna, Margit; Raik, Jaan; Ubar, Raimund-Johannes Scientific proceedings of Riga Technical University. 7. seria, Telecommunications and electronics 2001 / p. 91-94 : ill

Parallel X-fault simulation with critical path tracing technique [Electronic resource]

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur DATE 10 : Design, Automation & Test in Europe : Dresden, Germany, 8-12 March, 2010 2010 / p. 879-884 [CD-ROM] https://www.researchgate.net/publication/221341788_Parallel_X-fault_simulation_with_critical_path_tracing_technique

PASCAL : timing SCA resistant design and verification flow

Lai, Xinhui; Jenihhin, Maksim; Raik, Jaan; Paul, Kolin 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 239-242 : ill <https://doi.org/10.1109/IOLTS.2019.8854458>

Performance analysis of cosimulating processor core in VHDL and SystemC

Saif Abrar, Syed; Shyam Kiran A.; Jenihhin, Maksim; Raik, Jaan; Babu, C. Proceedings of the 2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 22–25 August 2013, Mysore, India 2013 / p. 563-568 : ill

Pooljuhtide tehnoloogia teeviit aastaks 2016 : kiipide tehnoloogia, projekteerimise ja testi tulevikuvision

Raik, Jaan A & A 2003 / 6, lk. 9-16

Preface

Ubar, Raimund-Johannes; Raik, Jaan; Vierhaus, Heinrich Theodor Design and test technology for dependable systems-on-chip 2011 / p. xxii-xxviii

Preface

Hollstein, Thomas; Raik, Jaan; Kostin, Sergei; Tšertov, Anton; O'Connor, Ian; Reis, Ricardo VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability, 24th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2016, Tallinn, Estonia, September 26-28, 2016 : Revised Selected Papers 2017 / p. V-VI https://link.springer.com/book/10.1007/978-3-319-67104-8_Conference_proceedings_at_Scopus_Article_at_Scopus

ProAct: Progressive Training for Hybrid Clipped Activation Function to Enhance Resilience of DNNs

Mousavi, Seyedhamidreza; Ahmadilivani, Mohammad Hasan; Raik, Jaan; Jenihhin, Maksim; Daneshtalab, Masoud arXiv.org 2024 / 12 p. : ill <https://doi.org/10.48550/arXiv.2406.06313>

Probabilistic analysis of CMOS physical defects in VLSI circuits for test coverage improvement

Blyzniuk, M.; Kazymyra, I.; Kuzmich, W.; Pleskacz, Witold A.; Raik, Jaan; Ubar, Raimund-Johannes Microelectronics reliability 2001 / p. 2023-2040 : ill <https://www.sciencedirect.com/science/article/pii/S0026271401000920>

Probabilistic equivalence checking based on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 423-428 : ill <https://ieeexplore.ieee.org/document/5783130>

Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany

2011 <https://www.computer.org/csdl/proceedings/ddecs/2011/12OmNvTBBbs>

Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia

2012 http://www.ester.ee/record=b2777270*est

PSL assertion checkers synthesis with ASM based HLS tool ABELITE

Jenihhin, Maksim; Baranov, Samary; Raik, Jaan; Tihomirov, Valentin LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / [6 p.] : ill <https://ieeexplore.ieee.org/document/6261251>

PSL assertion checking using temporally extended high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2009 / 6, p. 289-300 : ill https://pld.ttu.ee/home/maksim/phd_papers/%5B11%5D%20latw%2708.pdf

PSL assertion checking with temporally extended high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 49-54 : ill https://pld.ttu.ee/~maksim/phd_papers/%5B11%5D%20latw%2708.pdf

QoSInNoC: analysis of QoS-aware NoC architectures for mixed-criticality applications

Avramenko, Serhiy; Azad, Siavoosh Payandeh; Niazmand, Behrad; Raik, Jaan; Jenihhin, Maksim 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 67-72 : ill <https://doi.org/10.1109/DDECS.2018.00-10>

Rahvusvaheline süsteem-kiibil teaduskonverents Soomes - Tampere SoC Symposium 2003

Raik, Jaan A & A 2003 / 6, lk. 56

Ransomware attack as Hardware Trojan : a feasibility and demonstration study

Almeida, Felipe; Imran, Malik; Raik, Jaan; Pagliarini, Samuel Nascimento IEEE Access 2022 / p. 44827-44839 <https://doi.org/10.1109/ACCESS.2022.3168991> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Register-transfer level deductive fault simulation using decision diagrams

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 193-196 : ill

Rejuvenation of nanoscale logic at NBTI-critical paths using evolutionary TPG

Palermo, N.; Tihomirov, Valentin; Copetti, Thiago; Jenihhin, Maksim; Raik, Jaan; Kostin, Sergei 2015 16th Latin American Test Symposium (LATS 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2015.7102405>

Rejuvenation of NBTI-impacted processors using evolutionary generation of assembler programs

Pellerey, Francesco; Jenihhin, Maksim; Squillero, Giovanni; Raik, Jaan; Sonza Reorda, Matteo; Tihomirov, Valentin; Ubar, Raimund-Johannes 2016 IEEE 25th Asian Test Symposium : 21-24 November 2016, Hiroshima, Japan 2016 / p. 304-309 : ill <https://doi.org/10.1109/ATS.2016.57> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Reliability improvements for multiprocessor systems by health-aware task scheduling

Schmidt, Robert; Massoud, Rehab; Raik, Jaan; Garcia-Ortiz, Alberto; Drechsler, Rolf 2018 IEEE 24th International Symposium on On-Line Testing and Robust System Design (IOLTS 2018) : 2 - 4 July 2018, Spain 2018 / p. 247-250 : ill <http://dx.doi.org/10.1109/IOLTS.2018.8474101>

A rescue demonstrator for interdependent aspects of reliability, security and quality towards a complete EDA flow
Raik, Jaan; Jenihhin, Maksim 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2020 / p. 58 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9116424>

RESCUE EDA Toolset for interdependent aspects of reliability, security and quality in nanoelectronic systems design
Gürsoy, Cemil Cem; Cardoso Medeiros, Guilherme; Chen, Juanho; Balakrishnan, Aneesh; Lai, Xinhui; Bagbaba, Ahmet Cagri; Raik, Jaan; Jenihhin, Maksim DATE 2019 2019 / 1 p. : ill <https://doi.org/10.5281/zenodo.3362529> <https://past.date-conference.com/>

RESCUE: interdependent challenges of reliability, security and quality in nanoelectronic systems
Jenihhin, Maksim; Raik, Jaan 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2020 / art. 19690741 , 6 p <https://doi.org/10.23919/DATE48585.2020.9116558>

Research environment for teaching digital test
Ivask, Eero; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Synergies between Information and Automation : 49. Internationales Wissenschaftliches Kolloquium, 27.-30.9.2004, Technische Universität Ilmenau, Germany. Volume 2 2004 / p. 468-473 : ill https://pld.ttu.ee/dildis/publications/IWK'2004_res_inv.pdf

Research in digital design and test at Tallinn University of Technology
Ubar, Raimund-Johannes; Jervan, Gert; Jutman, Artur; Raik, Jaan; Ellervee, Peeter; Kruus, Margus Radioelectronics & informatics 2008 / p. 4-12 : ill <http://www.ewdtest.com/ri/%E2%84%96-1-40-january-march-2008/>

Research on digital system design and test at Tallinn University of Technology
Ubar, Raimund-Johannes; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert; Jutman, Artur; Kruus, Margus; Raik, Jaan Research in Estonia : present and future 2011 / p. 184-205 : ill

Reseeding using compaction of pre-generated LFSR sequences
Jutman, Artur; Aleksejev, Igor; Raik, Jaan; Ubar, Raimund-Johannes ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : 31st August to 3rd September 2008, Malta : conference guide 2008 / p. 215

Reseeding using compaction of pre-generated LFSR sub-sequences
Jutman, Artur; Aleksejev, Igor; Raik, Jaan; Ubar, Raimund-Johannes ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : Malta 2008 / p. 1290-1295 : ill <http://dx.doi.org/10.1109/ICECS.2008.4675096>

Resting EEG functional connectivity and graph theoretical measures for discrimination of depression
Orgo, Laura; Bachmann, Maie; Kalev, Kaia; Järvelaid, Mari; Raik, Jaan; Hinrikus, Hiie 4th IEEE EMBS International Conference on Biomedical and Health Informatics, BHI 2017 : Orlando, Florida, USA, 16-19 February 2017 / p. 389-392 : ill <https://doi.org/10.1109/BHI.2017.7897287>

RTL assertion mining with automated RTL-to-TLM abstraction
Ghasempouri, Tara; Danese, Alessandro; Pravadelli, Graziano; Bombieri, Nicola; Raik, Jaan Proceedings of the 2019 Forum on specification & Design Languages (FDL) 2019 / 8 p. : ill <https://doi.org/10.1109/FDL.2019.8876941>

RT-level identification of potentially testable initialization faults
Raik, Jaan; Fujiwara, Hideo; Krivenko, Anna The Ninth IEEE Workshop on RTL and High Level Testing (WRTL 2008), Sapporo, Japan 2008 / [6] p https://www.researchgate.net/publication/234032548_RT-level_identification_of_potentially_testable_initialization_faults

RT-level test point insertion for sequential circuits
Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes IWoTA 2004 : IEEE 1st International Workshop on Testability Assessment : November 2, 2004, Rennes, France : proceedings 2004 / p. 34-40 : ill <https://ieeexplore.ieee.org/document/1428412>

Ränioruga sideme katkestamine ohustab meie IT-sektorit
Raik, Jaan postimees.ee 2023 / Lk. 13 [Ränioruga sideme katkestamine ohustab meie IT-sektorit](#)

SAFFIRA: a Framework for Assessing the Reliability of Systolic-Array-Based DNN Accelerators
Taheri, Mahdi; Daneshtalab, Masoud; Raik, Jaan; Jenihhin, Maksim; Pappalardo, Salvatore; Jimenez, Paul; Deveautour, Bastien; Bosio, Alberto 27th International Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS) : 03-05 April 2024, Kielce, Poland 2024 / p. 19-24 : ill <https://doi.org/10.1109/DDECS60919.2024.10508925>

SCAAT: Secure cache alternative address table for mitigating cache logical side-channel attacks
Shalabi, Ameer; Ghasempouri, Tara; Ellervee, Peeter; Raik, Jaan 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / art. 20035366, p. 213-217 <https://doi.org/10.1109/DSD51259.2020.00043>

Scalable algorithm for structural fault collapsing in digital circuits
Ubar, Raimund-Johannes; Jürimägi, Lembit; Orasson, Elmet; Raik, Jaan 2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 5-7, 2015, Daejeon, Korea 2015 / p. 171-176 : ill

A scalable technique to identify true critical paths in sequential circuits

Ubar, Raimund-Johannes; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan Proceedings 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuit & Systems (DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 152-157 : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553>

A security verification template to assess cache architecture vulnerabilities

Ghasempouri, Tara; Raik, Jaan; Paul, Kolin; Reinbrecht, Cezar; Hamdioui, Said; Taouil, M. 2020 23rd International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), April 22nd – 24th 2020 Novi Sad, Serbia : Proceedings 2020 / art. 9095707, 6 p <https://doi.org/10.1109/DDECS50862.2020.9095707>

Sequential circuit test generation using decision diagram models

Raik, Jaan; Ubar, Raimund-Johannes Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 736-740: ill https://www.cs.york.ac.uk/rts/docs/SIGDA-Compendium-1994-2004/papers/1999/date99/pdf/11e_1.pdf

Sequential circuits BIST synthesis from signal specifications

Raik, Jaan; Jenihhin, Maksim; Adelbert, Rain Proceedings 23rd NORCHIP Conference : Oulu, Finland, 21-22 November 2005 2005 / p. 196-199 : ill <https://ieeexplore.ieee.org/document/1597023>

Sequential circuits BIST with status bit control

Raik, Jaan; Orasson, Elmet; Ubar, Raimund-Johannes Proceedings of the 11th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2004 : Szczecin, Poland, 24-26 June 2004 2004 / p. 507-510 : ill https://pld.ttu.ee/~raiub/files/aaaaa_pulk/MIXDES/jaan.pdf

Sequential test set compaction in LFSR reseeding

Jutman, Artur; Aleksejev, Igor; Raik, Jaan Design and test technology for dependable systems-on-chip 2011 / p. 476-493 : ill <https://ieeexplore.ieee.org/document/4738292>

A set of tools for estimating quality of built-in self-test in digital circuits

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the International Symposium on Signals, Circuits and Systems, Iasi (Romania), October 2-3, 1997 1997 / p. 362-365

Shared Structurally Synthesized BDDs for speeding-up parallel pattern simulation in digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Raik, Jaan 2015 Nordic Circuits and Systems Conference (NORCAS) : NORCHIP & International Symposium on System-on-Chip (SoC) : 1st IEEE NORCAS Conference : 26-28 October 2015, Oslo, Norway 2015 / [4] p. : ill <http://dx.doi.org/10.1109/NORCHIP.2015.7364406>

Side-channel attacks on triple modular redundancy schemes

Almeida, Felipe; Aksoy, Levent; Raik, Jaan; Pagliarini, Samuel Nascimento 2021 IEEE 30th Asian Test Symposium ATS 2021 : proceedings 2021 / p. 79-84 : ill <https://doi.org/10.1109/ATS52891.2021.00026> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Simulation of digital systems with high-level decision diagrams

Morawiec, Adam; Raik, Jaan; Ubar, Raimund-Johannes The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 35-38 : ill

Simulation-based hardware verification with high-level decision diagrams = Simuleerimisel põhinev riistvara verifitseerimine kõrgtaseme otsustusdiagrammide

Jenihhin, Maksim 2008 https://www.ester.ee/record=b2431332*est

Simulation-based verification with APRICOT framework using high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 13-16 : ill

SoC and NoC test technology [Electronic resource] : [PowerPoint presentation]

Raik, Jaan Design and Test Technology for Dependable Hardware/Software Systems : DEDIS/DAAD Summer Academy : BTU Cottbus, Sept. 1st-12th, 2008 2008 / [41] p. : ill. [CD-ROM]

SoCDep2 : a framework for dependable task deployment on many-core systems under mixed-criticality constraints

Azad, Siavoosh Payandeh; Niazmand, Behrad; Ellervee, Peeter; Raik, Jaan; Jervan, Gert; Hollstein, Thomas 2016 11th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC) : June 27-29, 2016, Tallinn, Estonia 2016 / [6] p. : ill <https://doi.org/10.1109/ReCoSoC.2016.7533903>

Software-based mitigation for memory address decoder aging

Kraak, D. H. P.; Gürsoy, Cemil Cem; Jenihhin, Maksim; Raik, Jaan LATS 2019 : 20th IEEE Latin American Test Symposium : Santiago, Chile, March 11th - 13th 2019 2019 / 6 p. : ill <https://doi.org/10.1109/LATW.2019.8704595>

Software-level TMR approach for on-board data processing in space applications

Janson, Karl; Treudler, Carl Johann; **Hollstein, Thomas**; **Raik, Jaan**; **Jenihhin, Maksim**; Fey, Goerschwin 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 147-152 : ill <https://doi.org/10.1109/DDECS.2018.00033>

Special session : approximation and fault resiliency of DNN accelerators

Ahmadilivani, Mohammad Hasan; Barbareschi, Mario; Barone, Salvatore; Bosio, Alberto; **Daneshtalab, Masoud**; Torca, Salvatore Della; Gavarini, Gabriele; **Jenihhin, Maksim**; **Raik, Jaan**; **Taheri, Mahdi** 2023 IEEE 41st VLSI Test Symposium (VTS) : proceedings 2023 / 10 p. : ill <https://doi.org/10.1109/VTS56346.2023.10140043> [Conference proceeding at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Special session: in-field ML-assisted intermittent fault localization and management in RISC-V SoCs

Selg, Hardi; **Shibin, Konstantin**; **Tsertov, Anton**; **Jenihhin, Maksim**; **Ellervee, Peeter**; **Raik, Jaan** 2024 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2024 <https://doi.org/10.1109/DFT63277.2024.10753541> [Article at Scopus](#)

Special session: reliability assessment recipes for DNN accelerators

Ahmadilivani, Mohammad Hasan; Bosio, Alberto; Deveautour, Bastien; Dos Santos, Fernando Fernandes; Guerrero-Balaguera, Juan-David; **Jenihhin, Maksim**; Kritikakou, Angeliki; Sierra, Robert Limas; **Raik, Jaan**; **Taheri, Mahdi** 42nd IEEE VLSI Test Symposium, VTS 2024 2024 / 11 p. : ill <https://doi.org/10.1109/VTS60656.2024.10538707> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

SPICE-inspired fast gate-level computation of NBTI-induced delays in nanoscale logic

Kostin, Sergei; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 223-228 : ill

SSBDD model : advantageous properties and efficient simulation algorithms

Raik, Jaan; **Jutman, Artur**; **Ubar, Raimund-Johannes** ETW'02 : 7th IEEE European Test Workshop, Gorfu Greece, May 26-29, 2002 : informal digest 2002 / p. 345-346 : ill

SSBDDs : advantageous model and efficient algorithms for digital circuit modeling, simulation & test

Jutman, Artur; **Raik, Jaan**; **Ubar, Raimund-Johannes** 5th International Workshop on Boolean Problems : September 19-20, 2002, Freiberg (Sachsen) : proceedings 2002 / p. 157-166 : ill

SSBDDs and double topology for multiple fault reasoning

Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14-17, 2012 2012 / p. 23-28 <https://www.semanticscholar.org/paper/SSBDDs-and-Double-Topology-for-Multiple-Fault-Ubar-Kostin/8ba04611a41768f0c277a4ba46ca666132fc2f65>

Structural decision diagrams in digital test : theory and applications

Ubar, Raimund-Johannes; **Raik, Jaan**; **Jenihhin, Maksim**; **Jutman, Artur** 2024 <https://doi.org/10.1007/978-3-031-44734-1> https://www.eester.ee/record=b5734441*est

Structural fault collapsing by superposition of BDDs for test generation in digital circuits

Ubar, Raimund-Johannes; **Mironov, Dmitri**; **Raik, Jaan**; **Jutman, Artur** Proceedings of the Eleventh International Symposium on Quality Electronic Design ISQED 2010 : March 22-24, 2010 San Jose, California USA 2010 / p. 250-257 : ill <https://ieeexplore.ieee.org/document/5450451>

Structurally synthesized binary decision diagrams

Jutman, Artur; Peder, Ahti; **Raik, Jaan**; Tombak, Mati; **Ubar, Raimund-Johannes** Boolean Problems : 6th International Workshop : September 23-24, 2004, Freiberg 2004 / p. 271-278 : ill

Structurally synthesized multiple input BDDs for simulation of digital circuits

Ubar, Raimund-Johannes; **Mironov, Dmitri**; **Raik, Jaan**; **Jutman, Artur** 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunisia, 13-19 December, 2009 2009 / p. 451-454 : ill <http://dx.doi.org/10.1109/ICECS.2009.5410895>

Structurally synthesized multiple input BDDs for speeding up logic-level simulation of digital circuits

Mironov, Dmitri; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** 13th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2010 : Lille, France, 1-3 September 2010 : proceedings 2010 / p. 658-663 : ill <https://ieeexplore.ieee.org/document/5615526>

Surrogate data method requires end-matched segmentation of electroencephalographic signals to estimate non-linearity

Päeske, Laura; **Bachmann, Maie**; **Pöld, Toomas**; Oliveira, Sara Pereira Mendes de; Lass, Jaanus; **Raik, Jaan**; **Hinrikus, Hiie** Frontiers in physiology 2018 / 1350 ; 9 p. : ill <https://doi.org/10.3389/FPHYS.2018.01350> [Journal metrics at Scopus](#) [Article at Scopus](#)

Survey on architectural attacks : a unified classification and attack model

Ghasempouri, Tara; Raik, Jaan; Reinbrecht, Cezar; Hamdioui, Said; Hamdioui, Said ACM Computing Surveys 2023 / art. 42
<https://doi.org/10.1145/3604803> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Süvatehnoloogiate alternatiivsed arengutrajektoorid ja nende tähendus Eestile : lõpparuanne

Koppel, Kaupo; Kuusik, Alar; Arrak, Kadri; **Raik, Jaan; Niidu, Allan;** Kõks, Kerttu-Liis; **Lahtvee, Petri-Jaan** 2023
<https://media.voog.com/0000/0037/5345/files>

Synthesis of high-level decision diagrams for functional test pattern generation

Ubar, Raimund-Johannes; Raik, Jaan; Karputkin, Anton; Tombak, Mati Proceedings of the 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009 : Lodz, Poland, 25-27 June, 2009 2009 / p. 519-524 : ill

Synthesis of multiple fault oriented test groups from single fault test sets [Electronic resource]

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan 2013 8th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS) : 26-28 March 2013, Abu Dhabi, UAE 2013 / p. 36-41 : ill [CD-ROM]

A systematic literature review on hardware reliability assessment methods for deep neural networks

Ahmadilivani, Mohammad Hasan; Taheri, Mahdi; Raik, Jaan; Daneshtalab, Masoud; Jenihhin, Maksim ACM Computing Surveys 2024 / art. 141, 39 p. : ill <https://doi.org/10.1145/3638242> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Systematic review of fault tolerant techniques in underwater sensor networks

Vihman, Lauri; Kruusmaa, Maarja; Raik, Jaan Sensors 2021 / art. 3264 <https://doi.org/10.3390/s21093264> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

SystemC-based loose models : RTL abstraction for design understanding

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan Workshop on Design Automation for Understanding Hardware Designs DUHDe 2015 : Grenoble, March 13, 2015 2015 / p. 1-6

SystemC-based loose models for simulation speed-up by abstraction of RTL IP cores

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 71-74 : ill
<http://dx.doi.org/10.1109/DDECS.2015.39>

zamiaCAD : open source platform for advanced hardware design

Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan DATE 2011 University Booth : Design Automation and Test in Europe : Grenoble, France, March 14-18, 2011 2011 / [2] p.: ill

zamiaCAD : understand, develop and debug hardware designs

Jenihhin, Maksim; Tihomirov, Valentin; Saif Abrar, Syed; Raik, Jaan; Bartsch, Günter DUHDe : 1st Workshop on Design Automation for Understanding Hardware Designs : March 28, 2014 : Friday Workshop at DATE 2014, Dresden, Germany 2014 / p. 1-6

Zero-memory-overhead clipping-based fault tolerance for LSTM deep neural networks

Parchekani, Bahram; Nazari, Samira; **Ahmadilivani, Mohammad Hasan; Azarpeyvand, Ali; Raik, Jaan; Ghasempouri, Tara; Daneshtalab, Masoud** 37th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, Harwell, Oxfordshire, Didcot, UK, October 8th - 10th, 2024 2024 / 4 p. : ill <https://doi.org/10.1109/DFT63277.2024.10753533> [Conference proceedings at Scopus](#) [Article at Scopus](#)

Targeting conditional operations in sequential test pattern generation

Raik, Jaan; Ubar, Raimund-Johannes 9th European Test Symposium : ETS'04 : Congress Center, Ajaccio, Corsica, France, May 23-26, 2004 2004 / p. 17-18 : ill
https://www.researchgate.net/publication/239717327_Targeting_Conditional_Operations_in_Sequential_Test_Pattern_Generation

Teaching advanced test issues in digital electronics

Ubar, Raimund-Johannes; Orasson, Elmet; Raik, Jaan; Wuttke, Heinz-Dietrich Proceedings of the 6th IEEE International Conference on Information Technology Based Higher Education and Training : ITHET : July 7-9, 2005, Juan Dolio, Dominican Republic 2005 / p. S2B-1 - S2B-6 : ill <http://dx.doi.org/10.1109/ITHET.2005.1560318>

Teaching diagnostic modeling of digital systems with decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Raik, Jaan; Mironov, Dmitri; Evartson, Teet; Orasson, Elmet; Aarna, Margit; Wuttke, Heinz-Dietrich Proceedings of 12th IASTED International Conference on Computers and Advanced Technology in Education - CATE 2009 : St. Thomas, US, November 22-24, 2009 2009 / p. 1-6. [CD-ROM]

Teaching research in the laboratory using diagnosis environment for digital systems

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan; Aarna, Margit; Brik, Marina; Wuttke, Heinz-Dietrich 2009 EAAEE annual conference : 20th Annual Conference of the European Association for Education in Electrical and Information Engineering : Valencia, Spain, June 22-24, 2009 / p. 280-283 <https://ieeexplore.ieee.org/document/5335462>

Teaching test and design for testability with TURBO-TESTER software

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 3rd Workshop on Mixed Design of Integrated Circuits and Systems, Lodz, May 1996 1996 / p. 589-594

Teadlase aju otsib vigu unes : [intervjuu Jaan Raigiga]

Raik, Jaan; Ideon, Argo Eesti Ekspress 2004 / 16. det., lk. A18-A19 : fot <https://ekspress.delfi.ee/artikkel/69048013/teadlase-aju-otsib-vigu-oosel-unes>

Teaduskonverentsi korraldamine Eestis nõuab paar aastat eeltööd : [intervjuu Jaan Raigiga]

Raik, Jaan; Kiviorg, Kristo Äripäev 2006 / 2. märts, Konverentsiturism, lk. 3

Techniques for automated localization and correction of design errors

Raik, Jaan CREDES Summer School : Dependable Systems Design : handouts 2011 / p. 107-118 : ill

Techniques for robust routing, communication and computation in multiprocessor systems = Robustse marsruutimise, side ja arvutuse tehnikad mitmeprotsessorilistes süsteemides

Janson, Karl 2021 https://www.ester.ee/record=b5396084*est <https://digikogu.taltech.ee/et/Item/c9091d5c-dcd8-4b21-95a7-84ead85241e6>
<https://doi.org/10.23658/taltech.3/2021>

Tehnikaülikooli teadurid teevad mikrokiipide vallas ajalugu : [arvutitehnika instituudi vanemteadur Jaan Raik jagab selgitusi]

Tooming, Urmas; **Raik, Jaan** Postimees 2009 / 28. juuli, lk. 7 : fot <https://majandus.postimees.ee/146505/tehnikaulikooli-teadurid-teevad-mikrokiipide-vallas-ajalugu>

Temporally extended high-level decision diagrams for PSL assertions simulation

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings : Thirteenth IEEE European Test Symposium : ETS 2008 : 25-29 May 2008, Verbania, Italy 2008 / p. 61-68 : ill <https://ieeexplore.ieee.org/document/4556029>

10th IEEE European Test Symposium

Ubar, Raimund-Johannes; Prinetto, Paolo; **Raik, Jaan** IEEE journal of design & test of computers 2005 / p. 480-481 : phot
<http://dx.doi.org/10.1109/MDT.2005.106>

Tere, tenuur!

Raik, Jaan Mente et Manu 2017 / lk. 4-5 : fot https://www.ttu.ee/public/m/mente-et-manu/MM_05_2017/mobile/index.html
https://artiklid.elnet.ee/record=b2826986*est

Test configurations for diagnosing faulty links in NoC switches

Raik, Jaan; Ubar, Raimund-Johannes; Govind, Vineeth 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 29-34 : ill <http://dx.doi.org/10.1109/ETS.2007.41>

Test configurations for diagnosing faulty links in NoC switches

Raik, Jaan; Ubar, Raimund-Johannes; Govind, Vineeth Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuseum 2007 / lk. 33-37 : ill

Test cover calculation in digital systems with word-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina Вестник Томского государственного университета 2002 / с. 315-319 : ил

Test development and deployment tool-set for mixed-signal and digital devices

Mellik, Andres; Raik, Jaan BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 163-166 : ill

Test generation with structurally synthesized BDD models

Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 5th Electronic Devices and Systems Conference, Brno, June 11-12, 1998 1998 / p. 66-68

Test set minimization using bipartite graphs

Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 175-178: ill

Test synthesis from register-transfer level descriptions

Raik, Jaan; Paomets, Priidu BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 311-314: ill

Testability analysis for efficient register-transfer level test generation [Electronic resource]

Nõmmeots, Tanel; Raik, Jaan; Ubar, Raimund-Johannes 9th International Conference MIXDES 2002 : Mixed Design of Integrated Circuits and Systems, Wroclaw, Poland, 20-22 June 2002 2002 / [4] p. [CD-ROM]

Testability guided hierarchical test generation with decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Nõmmeots, Tanel 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 2002 / p. 265-271 <https://www.semanticscholar.org/paper/Testability-Guided-Hierarchical-Test-Generation-Ubar-Raik/c6301ac35d003c92f3867f26e2e75b87e1ad9b47>

Testing strategies for networks on chip

Ubar, Raimund-Johannes; Raik, Jaan Networks on chip 2003 / p. 131-152 : ill https://link.springer.com/chapter/10.1007/0-306-48727-6_7

Testing tools

Raik, Jaan Handbook of testing electronic systems 2005 / p. 373-378 : ill

Testing tools for training and education

Balaž, M.; Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 12th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2005 : Krakow, Poland, 22-25 June, 2005. Vol. 1 of 2 2005 / p. 671-676 : ill

Timing-critical path analysis with structurally synthesized BDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; Jenihhin, Maksim; Raik, Jaan; Olugbenga, Niyi-Leigh; Viies, Vladimir 2018 7th Mediterranean Conference on Embedded Computing (MECO) 2018 / 6 p. : ill <https://doi.org/10.1109/MECO.2018.8406051>

A tool for random test generation targeting high diagnostic resolution

Osimiry, Emmanuel Ovie; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes BEC 2016 : 2016 15th Biennial Baltic Electronics Conference : proceedings of the 15th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 3-5, 2016, Tallinn, Estonia 2016 / p. 79-82 : ill http://www.ester.ee/record=b2150914*est

Towards formal verification of cache access-based side-channel attacks

Niazmand, Behrad; Reinbrecht, Cezar; Raik, Jaan; Jervan, Gert; Sepulveda, Johanna Testmethoden und Zuverlässigkeit von Schaltungen und Systemen, TUZ 2019 2019 / 2 p. : tab <http://www.informatik.uni-bremen.de/tuz/2019>

Towards multidimensional verification : where functional meets non-functional

Jenihhin, Maksim; Lai, Xinhui; Ghasempouri, Tara; Raik, Jaan 2018 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC) : 30-31 October 2018, Tallinn, Estonia : proceedings in IEEE Xplore 2018 / 7 p. : ill <https://doi.org/10.1109/NORCHIP.2018.8573495>

Transition delay fault simulation with parallel critical path back-tracing and 7-valued algebra

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan Microprocessors and microsystems 2015 / p. 1130-1138 : ill <https://doi.org/10.1016/j.micpro.2015.05.003> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Triple fixed-point MAC unit for deep learning

Kerner, Madis; Tammemäe, Kalle; Raik, Jaan; Hollstein, Thomas Proceedings of the 2021 Design, Automation & Test in Europe (DATE 2021), 1-5 February 2021 : Virtual Conference 2021 / p. 1404-1407 <https://doi.org/10.23919/DATe51398.2021.9474020>

TTBist: a DfT tool for enhancing functional test for SoC

Hermann, K.; Raik, Jaan; Jenihhin, Maksim BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 191-194 : ill

Turbo tester - diagnostic package for research and training

Aarna, Margit; Ivask, Eero; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Ubar, Raimund-Johannes; Vislogubov, Vladislav; Wuttke, Heinz-Dietrich Radioelectronics and informatics 2003 / p. 69-73 : ill

Turbo tester : a CAD system for teaching digital test

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Microelectronics education : proceedings of the 2nd European Workshop held in Noordwijkerhout, The Netherlands, 14-15 May 1998 1998 / p. 287-290: ill https://link.springer.com/chapter/10.1007/978-94-011-5110-8_66

Ultra fast parallel fault analysis on structurally synthesized BDDs

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur 12th IEEE European Test Symposium ETS 2007 : 20-

24 May 2007, Freiburg, Germany : proceedings 2007 / p. 131-136 : ill <http://dx.doi.org/10.1109/ETS.2007.43>

Ultra-low latency NoC testing via pseudo-random test pattern compaction

Tatenguem, Herve; **Govind, Vineeth; Raik, Jaan** SoC 2012 : International Symposium on System-on-Chip 2012 : Tampere, Finland, October 11-12, 2012 2012 / 6 p. : ill <https://ieeexplore.ieee.org/document/6376370>

Understanding multidimensional verification : where functional meets non-functional

Lai, Xinhui; Balakrishnan, Aneesh; Lange, Thomas; Jenihhin, Maksim; Ghasempouri, Tara; Raik, Jaan; Alexandrescu, Dan Microprocessors and microsystems 2019 / art. 102867, 13 p. : ill <https://doi.org/10.1016/j.micpro.2019.102867> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Untestable fault identification in sequential circuits using model-checking

Raik, Jaan; Fujiwara, Hideo; **Ubar, Raimund-Johannes; Krivenko, Anna** 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 257-262 : ill <https://ieeexplore.ieee.org/document/4711554>

Untestable fault identification in sequential circuits using model-checking

Raik, Jaan; Fujiwara, Hideo; **Ubar, Raimund-Johannes; Krivenko, Anna** Proceedings of the 17th Asian Test Symposium ATS 2008 : November 24-27, 2008, Sapporo, Japan 2008 / p. 21-26 : ill <http://dx.doi.org/10.1109/ATS.2008.22>

Upgrading QoSinNoC : efficient routing for mixed-criticality applications and power analysis

Avramenko, Serhiy; **Azad, Siavoosh Payandeh;** Violante, Massimo; Niazmand, Behrad; **Raik, Jaan; Jenihhin, Maksim** Proceedings of the 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 8-10, 2018, Verona, Italy 2018 / p. 207-212 : ill <https://doi.org/10.1109/VLSI-SoC.2018.8644866>

Using constraint solver in Test Pattern Generation Tool

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 14-17 : ill

Using simulation statistics for bug localization in RTL designs

Tihhomirov, Valentin; Jenihhin, Maksim; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 107-110 : ill

Using test pattern generation tool decider in hardware verification

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 166-169 : ill

Uudne turvaline kiibitehnoloogia

Raik, Jaan Mente et Manu 2021 / lk. 32-33 : fot [Mente et Manu 2/2021](#)

Web-based environment for digital electronics test tools

Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes; Schneider, Andre Virtual Enterprises and collaborative networks : IFIP 18th World Computer Congress [and] TC5/WG5.5 - 5th Working Conference on Virtual Enterprises : 22-27 August 2004, Toulouse, France 2004 / p. 435-442 : ill https://link.springer.com/chapter/10.1007/1-4020-8139-1_46

Web-based framework for distributed remote laboratory in the field of digital system test

Ivask, Eero; Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 182-187 : ill <http://dx.doi.org/10.1109/EAEEIE.2008.4610183>

Web-based framework for parallel distributed test [Electronic resource]

Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 271-274 : ill. [CD-ROM] <https://ieeexplore.ieee.org/document/4538800>

Vector decision diagrams for simulation of digital systems

Ubar, Raimund-Johannes; Morawiec, Adam; **Raik, Jaan** DDECS'2000 2000 / p. 44-51

Verifying cache architecture vulnerabilities using a formal security verification flow

Ghasempouri, Tara; Raik, Jaan; Paul, Kolin; Reinbrecht, Cezar; Hamdioui, Said; Taouil, Mottaqiallah Microelectronics reliability 2021 / art. 114085 <https://doi.org/10.1016/j.microrel.2021.114085> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

VHDL based test generation system

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 5th Electronic Devices and Systems Conference, Brno, June 11-12, 1998 1998 / p. 145-148

VHDL design debug framework based on zamiaCAD

Tihhomirov, Valentin; Tšepurov, Anton; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill

VILAB test generation tools running under the MOSCITO system

Schneider, Andre; Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes VILAB User Forum : Győr, Hungary, 2001 2001 / [12] p

Ученый-компьютерщик: ограничения США на поставки чипов замедлят цифровое развитие Эстонии

rus.err.ee 2025 [Ученый-компьютерщик: ограничения США на поставки чипов замедлят цифровое развитие Эстонии](#)