

### **Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs**

**Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan** Microprocessors and microsystems 2020 / art. 103117, 12 p <https://doi.org/10.1016/j.micpro.2020.103117> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

### **Conditional fault collapsing in digital circuits with shared structurally synthesized BDDs [Online resource]**

**Jürimägi, Lembit; Ubar, Raimund-Johannes** BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p. : ill <https://doi.org/10.1109/BEC.2018.8600967>

### **Equivalent transformations of structurally synthesized BDDs and applications**

**Jürimägi, Lembit; Ubar, Raimund-Johannes; Viies, Vladimir** 2019 8th Mediterranean Conference on Embedded Computing (MECO) 2019 / 6 p. : ill <https://doi.org/10.1109/MECO.2019.8760283>

### **Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems**

**Ubar, Raimund-Johannes** Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 303-324 : ill <http://dx.doi.org/10.2298/FUEE1103303U>

### **Structurally synthesized multiple input BDDs for simulation of digital circuits**

**Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur** 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunisia, 13-19 December, 2009 2009 / p. 451-454 : ill <http://dx.doi.org/10.1109/ICECS.2009.5410895>

### **Timing-critical path analysis with structurally synthesized BDDs**

**Ubar, Raimund-Johannes; Jürimägi, Lembit; Jenihhin, Maksim; Raik, Jaan; Olugbenga, Niyi-Leigh; Viies, Vladimir** 2018 7th Mediterranean Conference on Embedded Computing (MECO) 2018 / 6 p. : ill <https://doi.org/10.1109/MECO.2018.8406051>

### **True path tracing in structurally synthesized BDDs for testability analysis of digital circuits**

**Ubar, Raimund-Johannes; Jürimägi, Lembit; Oyeniran, Adeboye Stephen; Jenihhin, Maksim** Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 492-499 : ill <https://doi.org/10.1109/DSD.2019.00077>