

Code compaction within CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 133-136 : ill

Customizable compression architecture for efficient configuration in CGRAs

Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter** 2014 IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines : FCCM 2014 : 11-13 May 2014, Boston, Massachusetts, USA : proceedings 2014 / p. 31 : ill

DyMeP : an infrastructure to support dynamic memory binding for runtime mapping in CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter**; Hemani, Ahmed; Tenhunen, Hannu; Plosila, Juha 28th International Conference on VLSI Design : held concurrently with 14th International Conference on Embedded Systems : 3-7 January 2015, Bangalore, India : proceedings 2015 / p. 547-552 : ill <https://doi.org/10.1109/VLSID.2015.98> Conference proceedings at Scopus Article at Scopus Article at WOS

DyMeP : an infrastructure to support dynamic memory binding for runtime mapping in CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter**; Hemani, Ahmed; Tenhunen, Hannu; Plosila, Juha Doctoral School in Information and Communication Technology : proceedings of doctoral session of BEC 2014 : October 6-8 2014, Laulasmaa 2014 / lk. 19-22 : ill

Morphable compression architecture for efficient configuration in CGRAs

Jafri, Syed Mohammad Asad Hassan; Tajammul, Muhammad Adeel; **Ellervee, Peeter** 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 42-49 : ill

Polymorphic configuration architecture for CGRAs

Jafri, Syed Mohammad Asad Hassan; **Tajammul, Muhammad Adeel**; Hermanni, Ahmed; Paul, Kolin; Plosila, Juha; **Ellervee, Peeter**; Tenhunen, Hannu IEEE transactions on Very Large Scale Integration (VLSI) Systems 2016 / p. 403-407 : ill <http://dx.doi.org/10.1109/TVLSI.2015.2402392>

TransMem : a memory architecture to support dynamic remapping and parallelism in low power high performance CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; Hermanni, Ahmed; **Ellervee, Peeter** 2016 26th International Workshop on Power and Timing Modeling, Optimization and Simulation : PATMOS 2016 : September, 21st to 23th 2016, Bremen, Germany : proceedings 2016 / p. 92-99 : ill <https://doi.org/10.1109/PATMOS.2016.7833431>