

A scalable model based RTL framework zamiaCAD for static analysis

Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Tihhomirov, Valentin 2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC) : October 7-10, 2012 Santa Cruz, USA Dream Inn, Santa Cruz, USA : [proceedings] 2012 / p. 171-176 : ill <https://www.semanticscholar.org/paper/A-scalable-model-based-RTL-framework-zamiaCAD-for-Tsepurov-Bartsch/d19eefa44f793621d537c06498784e06e0332fd2>

Abstraction of clock interface for conversion of RTL VHDL to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan 2014 IEEE International Advance Computing Conference (IACC) : February 21-22, 2014, Gurgaon, India 2014 / p. 50-55 : ill

Accelerating transient fault injection campaigns by using Dynamic HDL Slicing

Bagbaba, Ahmet Cagri; Jenihhin, Maksim; Raik, Jaan; Sauer, Christian 2019 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC), 29-30 October 2019, Helsinki, Finland : proceedings in IEEE Xplore 2019 / 7 p. : ill <https://doi.org/10.1109/NORCHIP.2019.8906932>

Accurate NBTI-induced gate delay modeling based on intensive SPICE simulations

Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 21-26 : ill

AdAM: Adaptive Approximate Multiplier for Fault Tolerance in DNN Accelerators

Taheri, Mahdi; Cherezova, Natalia; Nazari, Samira; Azarpeyvand, Ali; Ghasempouri, Tara; Daneshtalab, Masoud; Raik, Jaan; Jenihhin, Maksim IEEE transactions on device and materials reliability 2024 / p. 66-75 : ill <https://doi.org/10.1109/TDMR.2024.3523386>

AdAM: adaptive fault-tolerant approximate multiplier for edge DNN accelerators

Taheri, Mahdi; Cherezova, Natalia; Nazari, Samira; Rafiq, Ahsan; Azarpeyvand, Ali; Ghasempouri, Tara; Daneshtalab, Masoud; Raik, Jaan; Jenihhin, Maksim 2024 IEEE European Test Symposium (ETS): ETS 2024 : May 20-24, 2024, The Hague, Netherlands : proceedings 2024 <https://doi.org/10.1109/ETS61313.2024.10567161> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

An Accelerator-based architecture utilizing an efficient memory link for modern computational requirements

Yousefzadeh, Saba; Basharkhah, Katayoon; Raik, Jaan; Jenihhin, Maksim 2019 IEEE East-West Design & Test Symposium (EWDTS) 2019 / 6 p. : ill <https://doi.org/10.1109/EWDTS.2019.8884481>

An approach for PSL assertion coverage analysis with high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Shchenova, Tatjana Proceedings of IEEE East-West Design & Test Symposium (EWDTS'10) : St. Petersburg, Russia, September 17-20, 2010 2010 / p. 13-16 : ill <https://ieeexplore.ieee.org/document/5742048>

An approach for verification assertions reuse in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Fujiwara, Hideo; Ubar, Raimund-Johannes; Viilukas, Taavi Digest of papers : IEEE 11th Workshop on RTL and High Level Testing : WRTL'10 : December 5-6, 2010, Shanghai, China 2010 / p. 107-110 : ill

An optimization framework for dynamic pipeline management in computing systems

Naqvi, Syed Rameez; Zahid, Anjum; Sawalha, Lina; Jenihhin, Maksim Computers & electrical engineering 2019 / p. 242-258 : ill <https://doi.org/10.1016/j.compeleceng.2019.07.013> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Analyzing side-channel attack vulnerabilities at RTL

Lai, Xinhui; Jenihhin, Maksim 2023 IEEE 24th Latin American Test Symposium (LATS) 2023 / 2 p. : ill <https://doi.org/10.1109/LATS58125.2023.10154497>

Application of high-level decision diagrams for simulation-based verification tasks

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Estonian journal of engineering 2010 / 1, p. 56-77 : ill

Application specific true critical paths identification in sequential circuits

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan; Devadze, Sergei; Oyeniran, Adeboye Stephen 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 299-304 : ill <https://doi.org/10.1109/IOLTS.2019.8854442>

Applications of the open source HW design framework zamiaCAD

Tšepurov, Anton; Tihhomirov, Valentin; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p

Applying RIS-based communication for collaborative computing in a swarm of drones

Rahbari, Dadmehr; Alam, Muhammad Mahtab; Le Moullec, Yannick; Jenihhin, Maksim IEEE Access 2023 / p. 70093-70109 <https://doi.org/10.1109/ACCESS.2023.3293737> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

APPRAISER : DNN fault resilience analysis employing approximation errors

Taheri, Mahdi; Ahmadilivani, Mohammad Hasan; Jenihhin, Maksim; Daneshtalab, Masoud; Raik, Jaan 2023 26th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) 2023 / p. 124–127 : ill
<https://ddec2023.taltech.ee/> <https://doi.org/10.1109/DDECS57882.2023.10139468>

An approach for verification assertions reuse 2 in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Fujiwara, Hideo Journal of Shanghai Normal University : Natural Sciences 2010 / p. 441–447 : ill
https://www.researchgate.net/publication/240613999_An_Approach_for_Verification_Assertions_Reuse_in_RTL_Test_Pattern_Generation

Approaches to extra-functional verification of security and reliability aspects in hardware designs = Riistvaraprojektide turva- ja töökindlusaspektide ekstrasfunktsionaalse verifitseerimise lähenemisviisid

Lai, Xinhui 2022 <https://doi.org/10.23658/taltech.29/2022> <https://digikogu.taltech.ee/et/Item/cff1aeb9-b0b2-49ce-b81a-bfb9dc25fd56>
https://www.ester.ee/record=b5502807*est

APRICOT : a framework for teaching digital systems verification

Raik, Jaan; Jenihhin, Maksim; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes 19th EAAEIE Annual Conference : June 29–July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 172–177 : ill
<http://dx.doi.org/10.1109/EAAEIE.2008.4610181>

Assertion checking with PSL and high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Digest of papers IEEE 8th Workshop on RTL and High Level Testing : WRTL07 : October 12–13, 2007, Beijing, China 2007 / p. 105–110 : ill
https://pld.ttu.ee/~maksim/phd_papers/%5B12%5D%20wrtl%2707.pdf

Assessment of diagnostic test for automated bug localization

Tihhomirov, Valentin; Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3–5, 2013 : [proceedings] 2013 / [6] p. : ill

Automated design error debug using high-level decision diagrams and mutation operators

Raik, Jaan; Repinski, Urmas; Tšepurov, Anton; Hantson, Hanno; Ubar, Raimund-Johannes; Jenihhin, Maksim Microprocessors and microsystems 2013 / p. 505–513 : ill <https://doi.org/10.1016/j.micpro.2012.11.004> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Automated design error localization in RTL designs

Jenihhin, Maksim; Tšepurov, Anton; Tihhomirov, Valentin; Raik, Jaan; Hantson, Hanno; Ubar, Raimund-Johannes; Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich IEEE design & test of computers 2014 / p. 83–92 : ill
<https://doi.org/10.1109/MDAT.2013.2271420> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Automated identification of application-dependent safe faults in automotive systems-on-a-chips

Bagbaba, Ahmet Cagri; Augusto da Silva, Felipe; Sonza Reorda, Matteo; Hamdioui, Said; Jenihhin, Maksim; Sauer, Christian Electronics 2022 / art. 319 <https://doi.org/10.3390/electronics11030319> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

An automated method for mining high-quality assertion sets

Heidari Iman, Mohammad Reza; Raik, Jaan; Jenihhin, Maksim; Jervan, Gert; Ghasempouri, Tara Microprocessors and microsystems 2023 / art. 104773 <https://doi.org/10.1016/j.micpro.2023.104773> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Automated test bench generation for high-level synthesis flow ABELITE

Viilukas, Taavi; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Baranov, Samary Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2011) : Sevastopol, Ukraine, September 9–12, 2011 2011 / p. 13–16 : ill
<https://ieeexplore.ieee.org/document/6116601>

BASTION : board and SoC test instrumentation for ageing and no failure found

Jutman, Artur; Lotz, Christophe; Larsson, Erik; Sonza Reorda, Matteo; Jenihhin, Maksim; Raik, Jaan Proceedings of the 2017 Design, Automation & Test in Europe (DATE) : 27–31 March 2017, Swisstech, Lausanne, Switzerland 2017 / p. 115–120 : ill
<https://doi.org/10.23919/DATE.2017.7926968>

Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Microprocessors and microsystems 2020 / art. 103117, 12 p <https://doi.org/10.1016/j.micpro.2020.103117> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Can a HW development and research environment be convenient, scalable and free? zamiaCAD : open-source platform for hardware design and analysis : [invited talk]

Jenihhin, Maksim Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14–17, 2012 2012 / p. 548-549

Challenges of reliability assessment and enhancement in autonomous systems

Jenihhin, Maksim; Sonza Reorda, Matteo; **Balakrishnan, Aneesh**; Alexandrescu, Dan 2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2019) 2019 / 6 p <https://doi.org/10.1109/DFT.2019.8875379>

Code coverage analysis for concurrent programming languages using high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes Proceedings of the 12th European Workshop on Dependable Computing : EWDC 2009 : Toulouse, France, May 14-15, 2009 2009 / [4] p. : ill <https://hal.archives-ouvertes.fr/hal-00381559>

Code coverage analysis using high-level decision diagrams [Electronic resource]

Raik, Jaan; Reinsalu, Uljana; Ubar, Raimund-Johannes; **Jenihhin, Maksim**; Ellervee, Peeter 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 201-207 : ill. [CD-ROM] <https://ieeexplore.ieee.org/document/4538786>

Combining dynamic slicing and mutation operators for ESL correction

Repinski, Urmaz; Hantson, Hanno; **Jenihhin, Maksim**; Raik, Jaan; Ubar, Raimund-Johannes Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th-June 1st, 2012, Annecy, France 2012 / [6] p. : ill <https://ieeexplore.ieee.org/document/6233020>

Composing graph theory and deep neural networks to evaluate SEU type soft error effects

Balakrishnan, Aneesh; Lange, Thomas; Glorieux, Maximilien; Alexandrescu, Dan; **Jenihhin, Maksim** 9th Mediterranean Conference on Embedded Computing (MECO'2020), Budva, Montenegro, 8-11 June 2020 2020 <https://doi.org/10.1109/MECO49872.2020.9134279>

Comprehensive abstraction of VHDL RTL cores to ESL SystemC = Register-siirde taseme VHDL kirjelduste kompleksne abstraherimine süsteemitaseme SystemC mudeliteks

Abrar, Syed Saif 2016 http://www.estee.ee/record=b4564850*est

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Raik, Jaan; Rannaste, Anna; **Jenihhin, Maksim**; Viilukas, Taavi; Ubar, Raimund-Johannes; Fujiwara, Hideo Sixteenth IEEE European Test Symposium : 23-27 May 2011, Trondheim 2011 / p. 147-152

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Viilukas, Taavi; Raik, Jaan; Ubar, Raimund-Johannes; Rannaste, Anna; **Jenihhin, Maksim**; Fujiwara, Hideo Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 139-142 : ill

Constraint-based test pattern generation at the register-transfer level

Viilukas, Taavi; Raik, Jaan; **Jenihhin, Maksim**; Ubar, Raimund-Johannes; Krivenko, Anna Proceedings of the 13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 14-16, 2010, Vienna, Austria 2010 / p. 352-357 : ill <http://dx.doi.org/10.1109/DDECS.2010.5491752>

Cost-effective fault tolerance for CNNs using parameter vulnerability based hardening and pruning

Ahmadilivani, Mohammad Hasan; Mousavi, Seyedhamidreza; **Raik, Jaan**; Daneshtalab, Masoud; **Jenihhin, Maksim** 2024 IEEE 30th International Symposium on On-line Testing and Robust System Design (IOLTS) : IOLTS 2024 : July 03rd-05th 2024, Rennes, Brittany, France 2024 / 7 p <https://doi.org/10.1109/IOLTS60994.2024.10616072> [Article at Scopus](#) [Article at WOS](#)

CREDES Summer School : Dependable Systems Design : handouts

2011 http://www.estee.ee/record=b2891192*est

DeepAxe : a framework for exploration of approximation and reliability trade-offs in DNN accelerators

Taheri, Mahdi; Riazati, Mohamad; **Ahmadilivani, Mohammad Hasan**; **Jenihhin, Maksim**; Daneshtalab, Masoud; **Raik, Jaan**; Sjödin, Mikael; Lisper, Björn 2023 24th International Symposium on Quality Electronic Design (ISQED) 2023 / 8 p. : ill <https://doi.org/10.1109/ISQED57927.2023.10129353>

DeepVigor: Vulnerability Value RanGes and FactORs for DNNs' Reliability Assessment

Ahmadilivani, Mohammad Hasan; **Taheri, Mahdi**; **Raik, Jaan**; Daneshtalab, Masoud; **Jenihhin, Maksim** IEEE European Test Symposium (ETS) : Venice, Italy, 22-26 May 2023 : proceedings 2023 / 6 p. : ill <https://doi.org/10.1109/ETS56758.2023.10174133>

DeepVigor+: Scalable and Accurate Semi-Analytical Fault Resilience Analysis for Deep Neural Networks

Ahmadilivani, Mohammad Hasan; **Raik, Jaan**; Daneshtalab, Masoud; **Jenihhin, Maksim** arXiv.org 2024 / 14 p. : ill <https://doi.org/10.48550/arXiv.2410.15742>

Dependability evaluation in fault-tolerant systems with high-level decision diagrams

Ubar, Raimund-Johannes; Jervan, Gert; Raik, Jaan; Jenihhin, Maksim; Ellervee, Peeter Computer Science Meets Automation : 10-13 September 2007 : proceedings. Volume II 2007 / p. 147-152 : ill https://www.db-thueringen.de/receive/dbt_mods_00008864

Design error diagnosis using backtrace algorithm on decision diagrams

Repinski, Urmass; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

Designing reliable cyber-physical systems

Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; **Devadze, Sergei; Jenihhin, Maksim; Jutman, Artur; Raik, Jaan; Shibin, Konstantin** Languages, design methods, and tools for electronic system design : selected contributions from FDL 2016 2018 / p. 15-38 : ill https://doi.org/10.1007/978-3-319-62920-9_2 [Conference Proceedings at Scopus](#) [Article at Scopus](#)

Designing reliable cyber-physical systems : overview associated to the special session at FDL'16

Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; **Devadze, Sergei; Jenihhin, Maksim; Jutman, Artur; Raik, Jaan; Shibin, Konstantin** The 2016 Forum on Specification & Design Languages : proceedings : Bremen, Germany, September 14-16, 2016 2016 / [8] p. : ill <https://doi.org/10.1109/FDL.2016.7880382>

A DFT scheme to improve coverage of hard-to-detect faults in FinFET SRAMs

Cardoso Medeiros, Guilherme; **Gürsoy, Cemil Cem**; Fieback, Moritz; Wu, Lizhou; **Jenihhin, Maksim**; Taouil, Mottaqiallah; Hamdioui, Said 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE), 9-13 March 2020, Grenoble, France : proceedings 2020 / p. 792-797 <https://doi.org/10.23919/DATE48585.2020.9116278>

Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis

Hantson, Hanno; Repinski, Urmass; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / [6 p.] : ill <https://ieeexplore.ieee.org/document/6261234>

Diagnostic modeling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill https://www.researchgate.net/publication/344994231_Diagnostic_Modeling_of_Digital_Systems_with_Multi-Level_Decision_Diagrams

Diagnostic modeling of microprocessors with high-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Brik, Marina; Istenberg, Martin; Wuttke, Heinz-Dietrich BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 147-150 : ill

Diagnostic test generation for statistical bug localization using evolutionary computation

Gaudesi, Marco; **Jenihhin, Maksim; Raik, Jaan; Tihomirov, Valentin; Ubar, Raimund-Johannes** Applications of Evolutionary Computation : 17th European Conference, EvoApplications 2014, Granada, Spain, April 23-25, 2014 : revised selected papers 2014 / p. 425-436 : ill https://doi.org/10.1007/978-3-662-45523-4_35 [Conference proceeding at Scopus](#) [Article at Scopus](#) [Conference proceeding at WOS](#) [Article at WOS](#)

Early RTL analysis for SCA vulnerability in fuzzy extractors of memory-based PUF enabled devices

Lai, Xinhui; Jenihhin, Maksim; Selims, Georgios arXiv.org 2020 / 6 p. : ill <https://doi.org/10.48550/arXiv.2008.08409> <https://arxiv.org/abs/2008.08409>

Edge-to-Fog collaborative computing in a swarm of drones

Rahbari, Dadmehr; Alam, Muhammad Mahtab; Le Moullec, Yannick; Jenihhin, Maksim Advances in Model and Data Engineering in the Digitalization Era : MEDI 2021 International Workshops: DETECT, SIAS, CSMMML, BIOC, HEDA, Tallinn, Estonia, June 21-23, 2021 : proceedings 2021 / p. 78-87 https://doi.org/10.1007/978-3-030-87657-9_6 [Conference Proceedings at Scopus](#) [Article at Scopus](#)

EEG analyzer prototype based on FPGA

Jenihhin, Maksim; Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Ellervee, Peeter; Hinrikus, Hiie; Bachmann, Maie; Lass, Jaanus 7th International Symposium on Image and Signal Processing and Analysis (ISPA 2011) : September 4-6, 2011, Dubrovnik, Croatia : proceedings 2011 / p. 101-106 : ill <https://ieeexplore.ieee.org/document/6046588>

Efficient fault injection based on dynamic HDL slicing technique

Bagbaba, Ahmet Cagri; Jenihhin, Maksim; Raik, Jaan; Sauer, Christian 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 52-53 : ill <https://doi.org/10.1109/IOLTS.2019.8854419>

E-learning environment for WEB-based study of testing

Ubar, Raimund-Johannes; Jutman, Artur; Raik, Jaan; Devadze, Sergei; Jenihhin, Maksim; Aleksejev, Igor; Tšepurov, Anton; Tšertov, Anton; Kostin, Sergei; Orasson, Elmet; Wuttke, Heinz-Dietrich Proceedings of the 8th European Workshop on

Electronics design and testing of the CMS Fast Beam Condition Monitor for HL-LHC

Shibin, Konstantin; Auzinger, Georg; Bakhshiansohi, Hamed; Dabrowski, Anne; Dierlamm, Alexander; Dragicevic, Marko; Gholami, Asghar; Gomez, Gervasio; Guthoff, Moritz; Haranko, Mykta; Honma, Alan; **Jenihhin, Maksim** Journal of physics : conference series 2023 / p. 50-51 <https://doi.org/10.48550/arXiv.2410.14867>

Energy-efficient multi-fragment Markov model guided online model-based testing for MPSoC

Vain, Jüri; Tsiopoulos, Leonidas; Kharchenko, Vyacheslav; **Apneet Kaur; Jenihhin, Maksim; Raik, Jaan; Nömm, Sven** Green IT Engineering: Social, Business and Industrial Applications 2019 / p. 273-297 https://doi.org/10.1007/978-3-030-00253-4_12 [Article collection at Scopus](#) [Article at Scopus](#)

Enhancing fault resilience of QNNs by selective neuron splitting

Ahmadilivani, Mohammad Hasan; Taheri, Mahdi; Raik, Jaan; Daneshtalab, Masoud; Jenihhin, Maksim 2023 IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS) 2023 / 5 p. : ill <https://doi.org/10.1109/AICAS57966.2023.10168633>

Estonia : e-Design and EDA

Jenihhin, Maksim 50th DAC Global Forum 2013 / [2] p

Exploration of Activation Fault Reliability in Quantized Systolic Array-Based DNN Accelerators

Taheri, Mahdi; Cherezova, Natalia; Ansari, Mohammad Saeed; **Jenihhin, Maksim**; Mahani, Ali; **Daneshtalab, Masoud; Raik, Jaan** Proceedings of the Twenty Fifth International Symposium on Quality Electronic Design : ISQED 2024 2024 / 8 p. : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=10528372> <https://doi.org/10.1109/ISQED60706.2024.10528372> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Extensible open-source framework for translating RTL VHDL IP cores to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

Fast and fair computation offloading management in a swarm of drones using a rating-based federated learning approach

Rahbari, Dadmehr; Alam, Muhammad Mahtab; Le Moullec, Yannick; Jenihhin, Maksim IEEE Access 2021 / p. 113832-113849 <https://doi.org/10.1109/ACCESS.2021.3104117> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast identification of true critical paths in sequential circuits

Ubar, Raimund-Johannes; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan; Jürimägi, Lembit Microelectronics reliability 2018 / p. 252-261 : ill <https://doi.org/10.1016/j.microrel.2017.11.027> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

FORTUNE: A Negative Memory Overhead Hardware-Agnostic Fault Tolerance Technique in DNNs

Nazari, Samira; Taheri, Mahdi; Azarpeyvand, Ali; Afsharchi, Mohsen; Ghasempouri, Tara; Herglotz, Christian; Daneshtalab, Masoud; Jenihhin, Maksim 2024 IEEE 33rd Asian Test Symposium (ATS) 2024 / p. 1-6 : ill <https://doi.org/10.1109/ATS64447.2024.10915463> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

FP7 DIAMOND : design error diagnosis and correction success stories

Raik, Jaan; Jenihhin, Maksim; Könighofer, Robert European Test Symposium (ETS), 2013, Avignon, France 2013 / p. 1-6

FPGA-based implementation of EEG analyzer

Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Jenihhin, Maksim; Ellervee, Peeter DATE'11 Friday Workshop on "Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing" : Grenoble, France, March 2011 2011 / [1] p <https://www.microsoft.com/en-us/research/wp-content/uploads/2017/03/ellervee.pdf>

FSMD RTL design manipulation for clock interface abstraction

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 10-13 August 2015, Kerala, India 2015 / p. 463-468 : ill <http://dx.doi.org/10.1109/ICACCI.2015.7275652>

Gate-level graph representation learning : a step towards the improved stuck-at faults analysis

Balakrishnan, Aneesh; Alexandrescu, Dan; Jenihhin, Maksim; Lange, Thomas; Glorieux, Maximilien Proceedings of the Twenty Second International Symposium on Quality Electronic Design (ISQED) : Santa Clara, USA, 7-9 April 2021 2021 / p. 24-30 <https://doi.org/10.1109/ISQED51717.2021.9424256>

Gate-level modelling of NBTI-induced delays under process variations

Copetti, Thiago; Cardoso Medeiros, Guilherme; Bolzani Poehls, Leticia; Vargas, Fabian; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 75-80 : ill <http://dx.doi.org/10.1109/LATW.2016.7483343>

Generating directed tests for C programs using RTL ATPG

Raik, Jaan; Drenkhan, Tiia; Jenihhin, Maksim; Viilukas, Taavi; Karputkin, Anton; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the IEEE 13th Workshop on RTL and High Level Testing (WRTL'12) 2012 / p. 1-6

Hardware modeling for design verification and debug = Riistvara modelleerimine disaini verifitseerimise ja silumise jaoks
Tšepurov, Anton 2013 https://www.ester.ee/record=b2963501*est

Heterogeneous Approximation of DNN HW Accelerators based on Channels Vulnerability

Cherezova, Natalia; Pappalardo, Salvatore; Taheri, Mahdi; Ahmadilivani, Mohammad Hasan; Deveautour, Bastien; Bosio, Alberto; Raik, Jaan; Jenihhin, Maksim 2024 IFIP/IEEE 32nd International Conference on Very Large Scale Integration (VLSI-SoC) 2024 / 4 p. : ill <https://doi.org/10.1109/VLSI-SoC62099.2024.10767798> [Conference proceedings at Scopus](#) [Article at Scopus](#)

Hierarchical analysis of short defects between metal lines in CMOS IC

Pleskacz, Witold A.; Jenihhin, Maksim; Raik, Jaan; Rakowski, Michal; Ubar, Raimund-Johannes; Kuzmicz, Wieslaw Proceedings : 11th EUROMICRO Conference on Digital System Design : Architectures, Methods and Tools : (DSD 2008) : September 3-5, 2008, Parma, Italy 2008 / p. 729-734 : ill <https://ieeexplore.ieee.org/document/4669309>

Hierarchical calculation of malicious faults for evaluating the fault-tolerance

Ubar, Raimund-Johannes; Devadze, Sergei; Jenihhin, Maksim; Raik, Jaan; Jervan, Gert; Ellervee, Peeter Proceedings : Fourth IEEE International Symposium on Electronic Design, Test and Applications : [DELTA 2008] : 23-25 January 2008, Hong Kong, SAR, China 2008 / p. 222-227 : ill <https://ieeexplore.ieee.org/document/4459544>

Hierarchical identification of NBTI-critical gates in nanoscale logic

Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Hierarchical timing-critical paths analysis in sequential circuits

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan; Devadze, Sergei; Kostin, Sergei 2018 IEEE 28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS 2018) : 2 – 4 July 2018, Spain 2018 / 6 p. : ill <https://doi.org/10.1109/PATMOS.2018.8464176>

High-Level Combined Deterministic and Pseudo-exhaustive Test Generation for RISC Processors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan 2019 IEEE European Test Symposium (ETS) : ETS 2019, May 27-31, 2019, Baden-Baden, Germany : Proceedings 2019 / 6 p. : ill <https://doi.org/10.1109/ETS.2019.8791526>

High-level combined deterministic and pseudo-exhaustive test generation for RISC processors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Gürsoy, Cemil Cem; Raik, Jaan 2019 IEEE European Test Symposium (ETS) : proceedings 2019 / 6 p. : ill <https://doi.org/10.1109/ETS.2019.8791526>

High-Level Decision Diagram manipulations for code coverage analysis

Minakova, Karina; Reinsalu, Uljana; Tšepurov, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level decision diagram simulation for diagnosis and soft-error analysis

Raik, Jaan; Repinski, Urmass; Jenihhin, Maksim; Tšepurov, Anton Design and test technology for dependable systems-on-chip 2011 / p. 294-309 : ill <https://www.igi-global.com/chapter/high-level-decision-diagram-simulation/51406>

High-level decision diagrams based coverage metrics for verification and test

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes LATW 2009 : 10th IEEE Latin American Test Workshop : Buzios, Rio de Janeiro, Brazil, March 2-5, 2009 2009 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2009.4813792>

High-level design error diagnosis using backtrace on decision diagrams

Raik, Jaan; Repinski, Urmass; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton 28th Norchip Conference : Tampere, Finland, 15-16 November 2010 : conference program and papers 2010 / [4] p. : ill <http://dx.doi.org/10.1109/NORCHIP.2010.5669486>

High-level fault diagnosis in RISC processors with Implementation-Independent Functional Test

Oyeniran, Adeboye Stephen; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) : Nicosia, Cyprus : 04-06 July 2022 2022 / p. 32-37 <https://doi.org/10.1109/ISVLSI54635.2022.00019>

High-Level Implementation-Independent Functional Software-Based Self-Test for RISC Processors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Journal of electronic testing : theory and applications 2020 / p. 87-103 <https://doi.org/10.1007/s10836-020-05856-7>

Holistic IJTAG-based external and internal fault monitoring in UAVs

Ahmed, Foisal; Jenihhin, Maksim arXiv.org 2023 / 6 p. : ill <https://doi.org/10.48550/arXiv.2303.01816>

Hybrid BIST optimization for core-based systems with test pattern broadcasting

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Zebo DELTA 2004 : second IEEE International Workshop on Electronic Design, Test and Applications : 28-30 January 2004, Perth, Australia : proceedings 2004 / p. 3-8 : ill <https://ieeexplore.ieee.org/document/1409808>

Hybrid BIST time minimization for core-based systems with STUMPS architecture

Jervan, Gert; Eles, Petru; Peng, Zebo; Ubar, Raimund-Johannes; Jenihhin, Maksim 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems : 3-5 November 2003, Boston, Massachusetts : proceedings 2003 / p. 225-232 : ill <https://ieeexplore.ieee.org/document/1250116>

Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits

Jenihhin, Maksim; Squillero, Giovanni; Tihomirov, Valentin; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill <https://doi.org/10.1007/s10836-016-5589-x> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Identification and rejuvenation of NBTI-critical paths in nanoscale logic circuits

Jenihhin, Maksim 1st International Workshop on Reliability and Aging in Forthcoming Electronic Systems : May 28-29, 2015, Cluj-Napoca, Romania 2015 / [1] p

Identifying NBTI-critical paths in nanoscale logic

Ubar, Raimund-Johannes; Vargas, Fabian; Jenihhin, Maksim; Raik, Jaan; Kostin, Sergei; Bolzani Poehls, Leticia 16th Euromicro Conference series on Digital System Design : DSD 2013 : proceedings : 4-6 September 2013, Santander, Spain 2013 / p. 136-141 : ill

Identifying untestable faults in sequential circuits using test path constraints

Viilukas, Taavi; Karputkin, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill <https://link.springer.com/article/10.1007/s10836-012-5312-5>

Implementation-independent functional test for transition delay faults in microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / p. 646-650 <https://doi.org/10.1109/DSD51259.2020.00105>

Implementation-independent functional test generation for RISC microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan VLSI-SoC 2019 : 27th IFIP/IEEE International Conference on Very Large Scale Integration : [proceedings] 2019 / p. 82-87 : ill <https://doi.org/10.1109/VLSI-SoC.2019.8920323>

Implementation-independent test generation for a large class of faults in RISC processor modules

Jenihhin, Maksim; Oyeniran, Adeboye Stephen; Raik, Jaan; Ubar, Raimund-Johannes 24th Euromicro Conference on Digital System Design (DSD) 2021 <https://doi.org/10.1109/DSD53832.2021.00090>

An iterative approach to test time minimization for parallel hybrid BIST architecture

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Z. 5th IEEE Latin-American Test Workshop - LATW 2004 : Cartagena, Colombia, 2004 : digest of papers 2004 / p. 98-103 : ill <https://www.ida.liu.se/labs/eslab/publications/pap/db/latw04.pdf>

An iterative approach to test time minimization for parallel hybrid BIST architectures

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Z. System-on-Chip Conference 2004 : Bastad, Sweden 2004 / p. ? <https://www.ida.liu.se/labs/eslab/publications/pap/db/latw04.pdf>

JÄNES : a NAS framework for ML-based EDA applications

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems 2021 <https://doi.org/10.1109/DFT52944.2021.9568321>

Kas tehisintellekt on väikeriigi demokraatia ja julgeoleku tugi või oht?

Vaaks, Eveliis Trialoog 2025 <https://trialoog.taltech.ee/kas-tehisintellekt-on-vaikeriigi-demokraatia-ja-julgeoleku-tugi-voi-oht/>

Keynote: cost-efficient reliability for Edge-AI chips

Jenihhin, Maksim; Taheri, Mahdi; Cherezova, Natalia; Ahmadilivani, Mohammad Hasan; Selg, Hardi; Jutman, Artur; Shibin, Konstantin; Tsertov, Anton; Devadze, Sergei; Kodamanchili, Rama Mounika; Rafiq, Ahsan; Raik, Jaan; Daneshtalab, Masoud 2024 IEEE 25th Latin American Test Symposium (LATS) 2024 / 2 p <https://doi.org/10.1109/LATS62223.2024.10534610> [Article at Scopus](#)

Layout to logic defect analysis for hierarchical test generation

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Pleskacz, Witold A.; Rakowski, Michal Proceedings of the 2007 IEEE Workshop on Design and Diagnostic Circuits and Systems : April 11-13, 2007, Krakow, Poland 2007 / p. 35-40 : ill <http://dx.doi.org/10.1109/DDECS.2007.4295251>

Localization of bugs in processor designs using zamiaCAD framework

Tšepurov, Anton; Tihhomirov, Valentin; Jenihhin, Maksim; Raik, Jaan 13th International Workshop on Microprocessor Test and Verification (MTV 2012) Common Challenges and Solutions : Austin, USA, December 10–12, 2012 2012 / p. 1-6 <https://ieeexplore.ieee.org/document/6519733>

Measuring and identifying aging-critical paths in FPGAs

Pfeifer, Petr; **Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes;** Pliva, Zdenek MEDIAN 2015 : the 4th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : March 13, 2015, Grenoble, France 2015 / p. 56-61 : ill

A methodology for automated mining of compact and accurate assertion sets

Heidari Iman, Mohammad Reza; Raik, Jaan; Jenihhin, Maksim; Jervan, Gert; Ghasempouri, Tara 2021 IEEE Nordic Circuits and Systems Conference (NorCAS) : Oslo, Norway, October 26-27 2021 / 7 p. : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&number=9599865> <https://doi.org/10.1109/NorCAS53631.2021.9599865>

Methods for reliability assessment and enhancement of deep neural networks hardware accelerators =

Süvanärvivõrkude riistvara kiirendite töökindluse hindamine ja täiustamine

Taheri, Mahdi 2025 https://www.ester.ee/record=b5728368*est <https://digikogu.taltech.ee/et/Item/9cf79768-17bc-44ec-a828-e4ccf6cf93f1> <https://doi.org/10.23658/taltech.4/2025>

Methods to optimize functional safety assessment for automotive integrated circuits = Meetodid autotööstuse kiipide funktsionaalse ohutuse hindamise optimeerimiseks

Bagbaba, Ahmet Cagri 2022 <https://doi.org/10.23658/taltech.9/2022> <https://digikogu.taltech.ee/et/Item/58b0b89d-b1ba-4a73-ba53-850910d697b5> https://www.ester.ee/record=b5491885*est

Mixed hierarchical-functional fault models for targeting sequential cores

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Jenihhin, Maksim Journal of systems architecture 2008 / 3/4, p. 465-477 : ill <https://www.sciencedirect.com/science/article/abs/pii/S1383762107001166>

Mixed-level identification of fault redundancy in microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Gürsoy, Cemil Cem; Raik, Jaan LATS 2019 : 20th IEEE Latin American Test Symposium : Santiago, Chile, March 11th - 13th 2019 2019 / 6 p. : ill <https://doi.org/10.1109/LATW.2019.8704591>

ML-based online design error localization for RISC-V implementations

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter; Raik, Jaan 2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS) : IOLTS 2023 : July 3rd-5th, 2023, Platania, Chania (Crete), Greece : proceedings 2023 / 7 p. <https://doi.org/10.1109/IOLTS59296.2023.10224864>

MLC: a machine learning based checker for soft error detection in embedded processors

Nosrati, Nooshin; **Jenihhin, Maksim;** Navabi, Zainalabedin Proceedings - 2022 IEEE 28th International Symposium on On-Line Testing and Robust System Design, IOLTS 2022 2022 / Code 183305 <https://doi.org/10.1109/IOLTS56730.2022.9897309> [Article at Scopus](#) [Article at WOS](#)

Modeling for multi-view interference analysis of design aspects in MPSoC designs

Vain, Jüri; Apneet Kaur; Tsiopoulos, Leonidas; Raik, Jaan; Jenihhin, Maksim RESCUE 2017 : Workshop on Reliability, Security and Quality : ETS17 Fringe Workshop, May 25-26, 2017, Limassol, Cyprus 2017 / p. 1-6 <http://www.ets17.org.cy/workshop/rescue-workshop.html>

Modeling gate-level abstraction hierarchy using graph convolutional neural networks to predict functional de-rating factors

Balakrishnan, Aneesh; Lange, Thomas; Glorieux, Maximilien; Alexandrescu, Dan; **Jenihhin, Maksim** 2019 NASA/ESA conference on adaptive hardware and systems AHS 2019 : proceedings 2019 / p. 72-78 : ill <https://doi.org/10.1109/AHS.2019.00007>

Modeling microprocessor faults on high-level decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Istenberg, Martin; Wuttke, Heinz-Dietrich DSN 2008 : supplemental : 2008 IEEE International Conference on Dependable Systems & Networks With FTCS & DCC (DSN) : June 24-27, 2008, Anchorage, Alaska 2008 / p. C17-C22 : ill. [CD-ROM] [https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08\(LAAS\)_files/Slides/WDSN08S-04-Ubar.pdf](https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08(LAAS)_files/Slides/WDSN08S-04-Ubar.pdf)

Modeling soft-error reliability under variability

Balakrishnan, Aneesh; Cardoso Medeiros, Guilherme; Gürsoy, Cemil Cem; Hamdioui, Said; **Jenihhin, Maksim;** Alexandrescu, Dan 2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 6-8 Oct. 2021 2021 / p. 1-6 <https://doi.org/10.1109/DFT52944.2021.9568295>

Multi-view modeling for MPSoC design aspects [Online resource]

Vain, Jüri; Apneet Kaur; Tsiopoulos, Leonidas; Raik, Jaan; Jenihhin, Maksim BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p.: ill <https://doi.org/10.1109/BEC.2018.8600986>

Mutation analysis for systemC designs at TLM

Guarnieri, Valerio; Bombieri, Nicola; Pravadelli, Graziano; Fummi, Franco; **Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes** 12th IEEE Latin American Test Workshop (LATW) : Porto de Galinhas, Brasil, 27-30 March 2011 2011 / [6] p <https://ieeexplore.ieee.org/document/5985925>

Mutation analysis with high-level decision diagrams

Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Tšepurov, Anton; Ubar, Raimund-Johannes; Guglielmo, Giuseppe di; Fummi, Franco LATW2010 : 11th Latin-American TestWorkshop, March 28-31, 2010, Punta del Este, Uruguay 2010 / [6] p. [CD-ROM] <https://ieeexplore.ieee.org/document/5550336>

Nanoelectronics aging mitigation using SSBDD based techniques and dedicated sensors

Ubar, Raimund-Johannes; Vargas, Fabian; **Jenihhin, Maksim; Raik, Jaan** MEDIAN Workshop on Circuit Reliability : Modeling and Monitoring, Rome, Italy, February 25, 2013 2013 / [1] p

New categories of Safe Faults in a processor-based Embedded System

Gürsoy, Cemil Cem; Jenihhin, Maksim; Oyeniran, Adeboye Stephen; Piumatti, Davide; **Raik, Jaan;** Sonza Reorda, Matteo; **Ubar, Raimund-Johannes** 2019 22nd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Cluj-Napoca, Romania : proceedings 2019 / 4 p. : ill <https://doi.org/10.1109/DDECS.2019.8724642>

A novel fault-tolerant logic style with self-checking capability

Taheri, Mahdi; Sheikhpour, Saeideh; Mahani, Ali; **Jenihhin, Maksim** Proceedings - 2022 IEEE 28th International Symposium on On-Line Testing and Robust System Design, IOLTS 2022 2022 / art. 183305 : ill <https://doi.org/10.1109/IOLTS56730.2022.9897818>

On antagonism between side-channel security and soft-error reliability in BNN inference engines

Lai, Xinhui; Lange, Thomas; **Balakrishnan, Aneesh;** Alexandrescu, Dan; **Jenihhin, Maksim** IFIP/IEEE 29th International Conference on Very Large Scale Integration (VLSI-SoC) 2021 / p. 1-6 <https://doi.org/10.1109/VLSI-SoC53125.2021.9606981>

On BTI aging rejuvenation in memory address decoders

Gürsoy, Cemil Cem; Kraak, Daniel; **Ahmed, Foisal;** Taouil, Mottaqiallah; **Jenihhin, Maksim;** Hamdioui, Said 2022 IEEE 23rd Latin American Test Symposium, LATS 2022 2022 / Code 184360 <https://doi.org/10.1109/LATS57337.2022.9936940>

On NBTI-induced aging analysis in IEEE 1687 reconfigurable scan networks

Damijanovic, Aleksa; Squillero, Giovanni; **Gürsoy, Cemil Cem; Jenihhin, Maksim** VLSI-SoC 2019 : 27th IFIP/IEEE International Conference on Very Large Scale Integration : [proceedings] 2019 / p. 335-340 : ill <https://doi.org/10.1109/VLSI-SoC.2019.8920313>

On reusability of verification assertions for testing

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Tšepurov, Anton BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 151-154 : ill

On reusability of verification assertions for testing

Jenihhin, Maksim; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 43-46 : ill

On test generation for microprocessors for extended class of functional faults

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan VLSI-SoC: New technology enabler : 27th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2019 Cusco, Peru, October 6-9, 2019 : Revised and Extended Selected Papers 2020 / p. 21-44 https://doi.org/10.1007/978-3-030-53273-4_Conference_proceedings_at_Scopus_Article_at_Scopus

On the combined use of HLDDs and EFSMs for functional ATPG

Di Guglielmo, Giuseppe; Fummi, Franco; **Jenihhin, Maksim;** Pravadelli, Graziano; **Raik, Jaan; Ubar, Raimund-Johannes** 5th IEEE East-West Design & Test Symposium EWDTS 2007 : September 7-10, 2007, Yerevan, Armenia 2007 / p. 503-508 : ill

On the reuse of TLM mutation analysis at RTL

Guarnieri, Valerio; **Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2012 / p. 435-448 : ill <https://link.springer.com/article/10.1007/s10836-012-5303-6>

On-chip sensors data collection and analysis for SoC health management

Shibin, Konstantin; Jenihhin, Maksim; Jutman, Artur; Devadze, Sergei; Tsertov, Anton 2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2023 / 6 p <https://doi.org/10.1109/DFT59622.2023.10313562>

Open-source framework and practical considerations for translating RTL VHDL to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan IP-SoC 2012 : IP Embedded System Conference & Exhibition : Grenoble, France, Dec. 4-5, 2012 2012 <https://www.design-reuse.com/articles/32685/translating-rtl-vhdl-to-systemc.html>

Optimization methodologies for Cycle-Accurate SystemC models converted from RTL VHDL

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan IP-SoC 2013 : IP embedded system conference and exhibition : Grenoble, France, November 6-7, 2013 2013

An optimized design of delay-and energy-efficient Booth multiplier

Rafiq, Ahsan; Jenihhin, Maksim e-Prime - Advances in Electrical Engineering, Electronics and Energy 2024 / art. 100698 <https://doi.org/10.1016/j.prime.2024.100698> [Journal metrics at Scopus](#) [Article at Scopus](#)

PASCAL : timing SCA resistant design and verification flow

Lai, Xinhui; Jenihhin, Maksim; Raik, Jaan; Paul, Kolin 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 239-242 : ill <https://doi.org/10.1109/IOLTS.2019.8854458>

Performance analysis of cosimulating processor core in VHDL and SystemC

Saif Abrar, Syed; Shyam Kiran A.; Jenihhin, Maksim; Raik, Jaan; Babu, C. Proceedings of the 2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 22–25 August 2013, Mysore, India 2013 / p. 563-568 : ill

ProAct: Progressive Training for Hybrid Clipped Activation Function to Enhance Resilience of DNNs

Mousavi, Seyedhamidreza; Ahmadilivani, Mohammad Hasan; Raik, Jaan; Jenihhin, Maksim; Daneshtalab, Masoud arXiv.org 2024 / 12 p. : ill <https://doi.org/10.48550/arXiv.2406.06313>

Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia

2012 http://www.ester.ee/record=b2777270*est

PSL assertion checkers synthesis with ASM based HLS tool ABELITE

Jenihhin, Maksim; Baranov, Samary; Raik, Jaan; Tihomirov, Valentin LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / [6 p.] : ill <https://ieeexplore.ieee.org/document/6261251>

PSL assertion checking using temporally extended high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2009 / 6, p. 289-300 : ill https://pld.ttu.ee/home/maksim/phd_papers/%5B11%5D%20latw%2708.pdf

PSL assertion checking with temporally extended high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 49-54 : ill https://pld.ttu.ee/~maksim/phd_papers/%5B11%5D%20latw%2708.pdf

PSL assertions based verification with HLDD tools

Jenihhin, Maksim Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 17-20 : ill

QoSInNoC: analysis of QoS-aware NoC architectures for mixed-criticality applications

Avramenko, Serhiy; Azad, Siavoosh Payandeh; Niazmand, Behrad; Raik, Jaan; Jenihhin, Maksim 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 67-72 : ill <https://doi.org/10.1109/DDECS.2018.00-10>

Rejuvenation of nanoscale logic at NBTI-critical paths using evolutionary TPG

Palermo, N.; Tihomirov, Valentin; Copetti, Thiago; Jenihhin, Maksim; Raik, Jaan; Kostin, Sergei 2015 16th Latin American Test Symposium (LATS 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2015.7102405>

Rejuvenation of NBTI-impacted processors using evolutionary generation of assembler programs

Pellerey, Francesco; Jenihhin, Maksim; Squillero, Giovanni; Raik, Jaan; Sonza Reorda, Matteo; Tihomirov, Valentin; Ubar, Raimund-Johannes 2016 IEEE 25th Asian Test Symposium : 21-24 November 2016, Hiroshima, Japan 2016 / p. 304-309 : ill <https://doi.org/10.1109/ATS.2016.57> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Reliability continuum and academic EDA

Jenihhin, Maksim 2nd International Training School on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN ISTS 2015) : Prague, Czech Republic, July 13-15, 2015 2015 / [1] p

Reliability-critical computation offloading in UAV swarms

Rahbari, Dadmehr; Ahmed, Faisal; Jenihhin, Maksim; Alam, Muhammad Mahtab; Le Moullec, Yannick IEEE Systems Journal 2024 / p. 1871-1882 <https://doi.org/10.1109/JSYST.2024.3432449> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Representing gate-level SET faults by multiple SEU faults on RT-level

Bagbaba, Ahmet Cagri; Jenihhin, Maksim; Ubar, Raimund-Johannes; Sauer, Christian 2020 IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS), 13-15 July 2020 : proceedings 2020 / art. 19889351, 6 p. : ill <https://doi.org/10.1109/IOLTS50870.2020.9159715>

RESCUE : cross-sectoral PhD training concept for interdependent reliability, security and quality

Vierhaus, Heinrich Theodor; **Jenihhin, Maksim; Sonza Reorda, Matteo** 2018 12th European Workshop on Microelectronics Education (EWME) : September 24–26, 2018 2018 / p. 45-50 : ill <https://doi.org/10.1109/EWME.2018.8629465>

A rescue demonstrator for interdependent aspects of reliability, security and quality towards a complete EDA flow

Raik, Jaan; Jenihhin, Maksim 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2020 / p. 58 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9116424>

RESCUE EDA Toolset for interdependent aspects of reliability, security and quality in nanoelectronic systems design

Gürsoy, Cemil Cem; Cardoso Medeiros, Guilherme; Chen, Juanho; Balakrishnan, Aneesh; Lai, Xinhui; Bagbaba, Ahmet Cagri; Raik, Jaan; Jenihhin, Maksim DATE 2019 2019 / 1 p. : ill <https://doi.org/10.5281/zenodo.3362529> <https://past.date-conference.com/>

RESCUE: interdependent challenges of reliability, security and quality in nanoelectronic systems

Jenihhin, Maksim; Raik, Jaan 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2020 / art. 19690741, 6 p <https://doi.org/10.23919/DATE48585.2020.9116558>

SAFFIRA: a Framework for Assessing the Reliability of Systolic-Array-Based DNN Accelerators

Taheri, Mahdi; Daneshtalab, Masoud; Raik, Jaan; Jenihhin, Maksim; Pappalardo, Salvatore; Jimenez, Paul; Deveautour, Bastien; Bosio, Alberto 2024 27th International Symposium on Design & Diagnostics of Electronic Circuits & Systems (DDECS) : 03-05 April 2024, Kielce, Poland 2024 / p. 19–24 : ill <https://doi.org/10.1109/DDECS60919.2024.10508925>

A scalable technique to identify true critical paths in sequential circuits

Ubar, Raimund-Johannes; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan Proceedings 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuit & Systems (DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 152-157 : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553>

Sequential circuits BIST synthesis from signal specifications

Raik, Jaan; Jenihhin, Maksim; Adelbert, Rain Proceedings 23rd NORCHIP Conference : Oulu, Finland, 21-22 November 2005 2005 / p. 196-199 : ill <https://ieeexplore.ieee.org/document/1597023>

Simulation-based hardware verification with high-level decision diagrams = Simuleerimisel põhinev riistvara verifitseerimine kõrgtaseme otsustusdiagrammide

Jenihhin, Maksim 2008 https://www.ester.ee/record=b2431332*est

Simulation-based verification with APRICOT framework using high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 13-16 : ill

Software-based mitigation for memory address decoder aging

Kraak, D. H. P.; **Gürsoy, Cemil Cem; Jenihhin, Maksim; Raik, Jaan** LATS 2019 : 20th IEEE Latin American Test Symposium : Santiago, Chile, March 11th - 13th 2019 2019 / 6 p. : ill <https://doi.org/10.1109/LATW.2019.8704595>

Software-level TMR approach for on-board data processing in space applications

Janson, Karl; Treudler, Carl Johann; Hollstein, Thomas; Raik, Jaan; Jenihhin, Maksim; Fey, Goerschwin 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 147-152 : ill <https://doi.org/10.1109/DDECS.2018.00033>

Special session : approximation and fault resiliency of DNN accelerators

Ahmadilivani, Mohammad Hasan; Barbareschi, Mario; Barone, Salvatore; Bosio, Alberto; Daneshtalab, Masoud; Torca, Salvatore Della; Gavarini, Gabriele; Jenihhin, Maksim; Raik, Jaan; Taheri, Mahdi 2023 IEEE 41st VLSI Test Symposium (VTS) : proceedings 2023 / 10 p. : ill <https://doi.org/10.1109/VTS56346.2023.10140043> [Conference proceeding at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Special session : AutoSoC - a suite of open-source automotive SoC benchmarks

Silva, Felipe Augusto da; **Bagbaba, Ahmet Cagri; Ruospo, Annachiara; Jenihhin, Maksim** 2020 IEEE 38th VLSI TEST SYMPOSIUM (VTS) - VTS 2020 : proceedings 2020 / 9 p. : ill <https://doi.org/10.1109/VTS48691.2020.9107599> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Special session: in-field ML-assisted intermittent fault localization and management in RISC-V SoCs

Selg, Hardi; Shibin, Konstantin; Tsertov, Anton; Jenihhin, Maksim; Ellervee, Peeter; Raik, Jaan 2024 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2024

<https://doi.org/10.1109/DFT63277.2024.10753541> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Special session: reliability assessment recipes for DNN accelerators

Ahmadilivani, Mohammad Hasan; Bosio, Alberto; Deveautour, Bastien; Dos Santos, Fernando Fernandes; Guerrero-Balaguera, Juan-David; Jenihhin, Maksim; Kritikakou, Angeliki; Sierra, Robert Limas; Raik, Jaan; Taheri, Mahdi 42nd IEEE VLSI Test Symposium, VTS 2024 2024 / 11 p. : ill <https://doi.org/10.1109/VTS60656.2024.10538707> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

<https://doi.org/10.1109/VTS60656.2024.10538707> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

SPICE-inspired fast gate-level computation of NBTI-induced delays in nanoscale logic

Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 223-228 : ill

Structural decision diagrams in digital test : theory and applications

Ubar, Raimund-Johannes; Raik, Jaan; Jenihhin, Maksim; Jutman, Artur 2024 <https://doi.org/10.1007/978-3-031-44734-1>

https://www.eester.ee/record=b5734441*est

A survey on UAV computing platforms : a hardware reliability perspective

Ahmed, Faisal; Jenihhin, Maksim Sensors 2022 / art. 6286 <https://doi.org/10.3390/s22166286> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

[Journal metrics at WOS](#) [Article at WOS](#)

A synthetic, hierarchical approach for modelling and managing complex systems' quality and reliability = Sünteetiline, hierarhiline lähenemine keerukate süsteemide kvaliteedi ja töökindluse modelleerimiseks ja haldamiseks

Balakrishnan, Aneesh 2022 <https://doi.org/10.23658/taltech.11/2022> <https://digikogu.taltech.ee/et/Item/a594d3ec-0e6b-4a78-819a-fe1f47992612>

A systematic literature review on hardware reliability assessment methods for deep neural networks

Ahmadilivani, Mohammad Hasan; Taheri, Mahdi; Raik, Jaan; Daneshtalab, Masoud; Jenihhin, Maksim ACM Computing Surveys 2024 / art. 141, 39 p. : ill <https://doi.org/10.1145/3638242> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

<https://doi.org/10.1145/3638242> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

SystemC-based loose models : RTL abstraction for design understanding

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan Workshop on Design Automation for Understanding Hardware Designs DUHDe 2015 : Grenoble, March 13, 2015 2015 / p. 1-6

SystemC-based loose models for simulation speed-up by abstraction of RTL IP cores

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 71-74 : ill

<http://dx.doi.org/10.1109/DDECS.2015.39>

zamiaCAD : open source platform for advanced hardware design

Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan DATE 2011 University Booth : Design Automation and Test in Europe : Grenoble, France, March 14-18, 2011 2011 / [2] p.: ill

zamiaCAD : shall we dance?

Jenihhin, Maksim Open Source Tools for Verification : DVClub 14 January 2013 2013 / 1 p

zamiaCAD : understand, develop and debug hardware designs

Jenihhin, Maksim; Tihhomirov, Valentin; Saif Abrar, Syed; Raik, Jaan; Bartsch, Günter DUHDe : 1st Workshop on Design Automation for Understanding Hardware Designs : March 28, 2014 : Friday Workshop at DATE 2014, Dresden, Germany 2014 / p. 1-6

TalTech panustab kosmosevaldkonda kiipide, päikesepaneelide ja satelliitidega

Normak, Liisu Kirke Trialoog 2025 <https://trialoog.taltech.ee/taltech-panustab-kosmosevaldkonda-kiipide-paikesepaneelide-ja-satelliitidega/>

Temporally extended high-level decision diagrams for PSL assertions simulation

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings : Thirteenth IEEE European Test Symposium : ETS 2008 : 25-29 May 2008, Verbania, Italy 2008 / p. 61-68 : ill <https://ieeexplore.ieee.org/document/4556029>

Test time minimization for hybrid BIST of core-based systems

Jervan, Gert; Eles, Petru; Peng, Zebo; Ubar, Raimund-Johannes; Jenihhin, Maksim 12th Asian Test Symposium (ATS 2003) : 17-19 November 2003, Xian, China 2003 / p. 318-325 : ill <https://link.springer.com/article/10.1007/s11390-006-0907-x>

Test time minimization for hybrid BIST of core-based systems

Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** Journal of computer science and technology 2006 / 6, p. 907-912 : ill <https://link.springer.com/article/10.1007/s11390-006-0907-x>

The validation of graph model-based, gate level low-dimensional feature data for machine learning applications

Balakrishnan, Aneesh; Lange, Thomas; Glorieux, Maximilien; Alexandrescu, Dan; **Jenihhin, Maksim** 2019 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC), 29-30 October 2019, Helsinki, Finland : proceedings in IEEE Xplore 2019 / 7 p <https://doi.org/10.1109/NORCHIP.2019.8906974>

Timing-critical path analysis with structurally synthesized BDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; **Jenihhin, Maksim**; Raik, Jaan; Olugbenga, Niyi-Leigh; Viies, Vladimir 2018 7th Mediterranean Conference on Embedded Computing (MECO) 2018 / 6 p. : ill <https://doi.org/10.1109/MECO.2018.8406051>

Towards multidimensional verification : where functional meets non-functional

Jenihhin, Maksim; Lai, Xinhui; Ghasempouri, Tara; Raik, Jaan 2018 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC) : 30-31 October 2018, Tallinn, Estonia : proceedings in IEEE Xplore 2018 / 7 p. : ill <https://doi.org/10.1109/NORCHIP.2018.8573495>

True path tracing in structurally synthesized BDDs for testability analysis of digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Oyeniran, Adeboye Stephen; **Jenihhin, Maksim** Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 492-499 : ill <https://doi.org/10.1109/DSD.2019.00077>

TTBist: a DfT tool for enhancing functional test for SoC

Hermann, K.; **Raik, Jaan**; **Jenihhin, Maksim** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 191-194 : ill

2018 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC) : 30-31 October 2018, Tallinn, Estonia : proceedings in IEEE Xplore [Online resource]

2018 <https://ieeexplore.ieee.org/xpl/conhome/8552599/proceeding>

Töökindla arvutusriistvara keskuse juht Maksim Jenihhin

Jenihhin, Maksim forte.delfi.ee 2024 [Töökindla arvutusriistvara keskuse juht Maksim Jenihhin](https://forte.delfi.ee/record=b1242496*est)

Tööstusdoktorantuur projektis RESCUE

Jenihhin, Maksim Mente et Manu 2017 / lk. 21 http://www.ester.ee/record=b1242496*est

Understanding fault-tolerance vulnerabilities in advanced SoC FPGAs for critical applications

Cherezova, Natalia; **Shibin, Konstantin**; **Jenihhin, Maksim**; Jutman, Artur Microelectronics reliability 2023 / art. 115010, 10 p. : ill <https://doi.org/10.1016/j.microrel.2023.115010> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Understanding multidimensional verification : where functional meets non-functional

Lai, Xinhui; **Balakrishnan, Aneesh**; Lange, Thomas; **Jenihhin, Maksim**; **Ghasempouri, Tara**; **Raik, Jaan**; Alexandrescu, Dan Microprocessors and microsystems 2019 / art. 102867, 13 p. : ill <https://doi.org/10.1016/j.micpro.2019.102867> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Universal mitigation of NBTI-induced aging by design randomization

Jenihhin, Maksim; Kamkin, Alexander; Navabi, Zainalabedin; Sadeghi-Kohan, Somayeh Proceedings of 2016 IEEE East-West Design & Test Symposium (EWDTS) : Yerevan, Armenia, October 14-17, 2016 2017 / [5] p. : ill <http://dx.doi.org/10.1109/EWDTS.2016.7807635>

Unsupervised recycled FPGA detection using symmetry analysis

Tarique, Tanvir Ahmad; **Ahmed, Faisal**; **Jenihhin, Maksim**; Ali, Liakot 12th International Conference on Electrical and Computer Engineering : ICECE 2022 2022 / p. 437-440 <https://doi.org/10.1109/ICECE57408.2022.10088856>

Upgrading QoS in NoC : efficient routing for mixed-criticality applications and power analysis

Avramenko, Serhiy; **Azad, Siavoosh Payandeh**; Violante, Massimo; Niazmand, Behrad; **Raik, Jaan**; **Jenihhin, Maksim** Proceedings of the 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 8-10, 2018, Verona, Italy 2018 / p. 207-212 : ill <https://doi.org/10.1109/VLSI-SoC.2018.8644866>

Using simulation statistics for bug localization in RTL designs

Tihhomirov, Valentin; **Jenihhin, Maksim**; **Raik, Jaan** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 107-110 : ill

Wafer-level die re-test success prediction using machine learning

Selg, Hardi; **Jenihhin, Maksim; Ellervee, Peeter** 21st IEEE Latin-American Test Symposium (LATS) 2020 : proceedings 2020 / 5 p
<https://doi.org/10.1109/LATS49555.2020.9093672>

VHDL design debug framework based on zamiaCAD

Tihhomirov, Valentin; Tšepurov, Anton; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill

Китайский ИИ сталкивается с ограничениями на Западе: введут ли их в Эстонии?

Karpi, A-M. rus.postimees.ee 2025 [Китайский ИИ сталкивается с ограничениями на Западе: введут ли их в Эстонии?](#)

Профессор TalTech: закон об ИИ стал первым комплексным инструментом для защиты прав граждан

Jenihhin, Maksim rus.err.ee 2025 [Профессор TalTech: закон об ИИ стал первым комплексным инструментом для защиты прав граждан](#)
[autor](#)

«Сейчас время больших перемен»: профессор TalTech приоткрыл завесу тайны развития ИИ в Эстонии

Grebneva, N.; **Jenihhin, Maksim** rus.postimees.ee 2025 [«Сейчас время больших перемен»: профессор TalTech приоткрыл завесу тайны развития ИИ в Эстонии](#)