

Acceleration of recursive data sorting over tree-based structures

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Sklyarov, Valery; Skliarova, Iuliia Elektronika ir elektrotehnika = Electronics and electrical engineering 2011 / p. 51-56 : ill <https://eejournal.ktu.lt/index.php/elt/article/view/612>

Address-based data processing over N-ary trees

Sklyarov, Valery; Skliarova, Iuliia; **Kruus, Margus; Mihhailov, Dmitri; Sudnitsõn, Aleksander** EuroCon 2013 : 01-04 July 2013, Zagreb, Croatia 2013 / p. 1790-1797 : ill

Analysis and comparison of attainable hardware acceleration in all programmable systems-on-chip

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; **Sudnitsõn, Aleksander** Euromicro Conference on Digital System Design : DSD 2015 : 26-28 August 2015, Funchal, Madeira, Portugal : proceedings 2015 / p. 345-352 : ill <http://dx.doi.org/10.1109/DSD.2015.45>

Application of extensible processing platforms for experiments with FPGA-based circuits

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; **Rjabov, Artjom; Sudnitsõn, Aleksander** MELECON 2014 : 2014 17th IEEE Mediterranean Electrotechnical Conference : 13-16 April 2014, Beirut, Lebanon 2014 / p. 467-471 : ill <https://doi.org/10.1109/MELCON.2014.6820579> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Application-specific hardware accelerator for implementing recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Proceedings of the IEEE International Conference on Field Programmable Technology (FPT'10) : Beijing, China Dec. 8-10, 2010 2010 / p. 269-272 : ill <https://ieeexplore.ieee.org/document/5681486>

Computing sorted subsets for data processing in communicating software/hardware control systems

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** International journal of computers communications & control 2016 / p. 126-141 : ill <https://doi.org/10.15837/ijccc.2016.1.1442> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Design of FPGA-based circuits using hierarchical finite state machines

Skliarova, Iuliia; Sklyarov, Valery; **Sudnitsõn, Aleksander** 2012 http://www.ester.ee/record=b2857138*est

Design space exploration in multi-level computing systems

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; **Sudnitsõn, Aleksander** CompSysTech'14 : 15th International Conference on Computer Systems and Technologies : Ruse, Bulgaria, June 27-28, 2014 2014 / p. 40-47 : ill <https://doi.org/10.1145/2659532.2659616> [Conference proceedings at Scopus](#) [Article at Scopus](#)

Fast data sort based on searching networks with ring pipeline

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Elektronika ir elektrotehnika = Electronics and electrical engineering 2016 / p. 58-62 : ill <https://doi.org/10.5755/j01.eie.22.4.15920> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast iterative circuits and RAM-based mergers to accelerate data sort in software/hardware systems

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** Proceedings of the Estonian Academy of Sciences 2017 / p. 323-335 : ill <https://doi.org/10.3176/proc.2017.3.07> http://www.ester.ee/record=b2355998*est [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast matrix covering in all programmable systems-on-chip

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** Elektronika ir elektrotehnika = Electronics and electrical engineering 2014 / p. 150-153 : ill <https://doi.org/10.5755/j01.eie.20.5.7116> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast processing of non-repeated values in hardware

Skliarova, Iuliia; Sklyarov, Valery; **Sudnitsõn, Aleksander** Elektronika ir elektrotehnika = Electronics and electrical engineering 2017 / p. 74-77 : ill <https://doi.org/10.5755/j01.eie.23.3.18336> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

FPGA-based accelerators for parallel data sort

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Applied computer systems 2014 / p. 53-63 : ill

FPGA-based systems in information and communication

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** AICT2011 : 5th International Conference on Application of Information and Communication Technologies : 12-14 October, Baku, Azerbaijan : conference proceedings 2011 / p. 551-555 https://www.researchgate.net/publication/254014990_FPGA-based_systems_in_information_and_communication

FPGA-based time and cost effective Hamming weight comparators for binary vectors

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander; Kruus, Margus** Proceedings : EUROCON 2015 : Salamanca, Spain, 8th-11th September 2015 / p. 328-333 : ill <http://dx.doi.org/10.1109/EUROCON.2015.7313700>

Hardware accelerators for information retrieval and data mining

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; **Sudnitsõn, Aleksander; Rjabov, Artjom** 2015 International Conference on Information and Communication Technology Research (ICTRC2015) : Abu Dhabi, United Arab Emirates, May 17-19, 2015 / p. 202-205 : ill <http://dx.doi.org/10.1109/ICTRC.2015.7156457>

Hardware implementation of recursive algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 53rd IEEE International Midwest Symposium on Circuits and Systems : Seattle, Washington, USA, August 1-4, 2010 : proceedings 2010 / p. 225-228
<https://ieeexplore.ieee.org/document/5548674>

Hardware implementation of recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 2011 International Conference on Electronic Devices, Systems and Applications (ICEDSA) : Kuala Lumpur, Malaysia, April 25-27, 2011 : [proceedings] 2011 / p. 33-38 : ill
<https://ieeexplore.ieee.org/document/5959040>

Hardware implementation of recursive sorting algorithms using tree-like structures and HFSM models = Rekursiivsete sortimisalgoritmide riistvaraline realiseerimine kasutades puulaadseid struktuure ja HFSM mudeleid

Mihhailov, Dmitri 2011 https://www.ester.ee/record=b2748823*est

Hardware/software co-design for programmable systems-on-chip

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; Rjabov, Artjom; **Sudnitsõn, Aleksander**; Cardoso, Cláudia 2014
http://www.ester.ee/record=b3087107*est

Hardware/software co-design in extensible processing platforms for combinatorial search algorithms

Skliarova, Iuliia; Sklyarov, Valery; **Rjabov, Artjom; Sudnitsõn, Aleksander** MELECON 2014 : 2014 17th IEEE Mediterranean Electrotechnical Conference : 13-16 April 2014, Beirut, Lebanon 2014 / p. 462-466 : ill <https://doi.org/10.1109/MELCON.2014.6820578>
[Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

High-performance hardware accelerators for sorting and managing priorities

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 313-318 : ill
<https://ieeexplore.ieee.org/document/5783103>

High-performance information processing in distributed computing systems

Sklyarov, Valery; **Rjabov, Artjom**; Skliarova, Iuliia; **Sudnitsõn, Aleksander** International journal of innovative computing, information and control 2016 / p. 139-160 : ill https://www.researchgate.net/publication/297047447_High-performance_information_processing_in_distributed_computing_systems [Journal metrics at Scopus](#) [Article at Scopus](#)

Implementation in FPGA of address-based data sorting

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 21st International Conference on Field Programmable Logic and Applications : FPL 2011 : Chania, Crete, Greece, 5-7 September 2011 2011 / p. 405-410 : ill
https://www.researchgate.net/publication/220760392_Implementation_in_FPGA_of_Address-Based_Data_Sorting

Implementation of address-based data sorting on different FPGA platforms

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14-17, 2012 2012 / p. 38-41
<https://www.semanticscholar.org/paper/Implementation-of-address-based-data-sorting-on-Mihhailov-Sudnitsõn/e9294d725ab92a2d2a51ccb44fc47e80798bc071>

Implementation of parallel operations over streams in extensible processing platforms

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS) : August 4-7, 2013, Columbus, Ohio : [proceedings] 2013 / p. 852-855 : ill
<https://doi.org/10.1109/MWSCAS.2013.6674783> [Conference Proceedings at Scopus](#) [Article at Scopus](#)

Implementation of sorting algorithms in reconfigurable hardware

Skliarova, Iuliia; Sklyarov, Valery; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2012 IEEE Mediterranean Electrotechnical Conference (MELECON 2012) : Yasmine Hammamet, Tunisia, March 25-28, 2012 2012 / p. 107-110 : ill
<https://ieeexplore.ieee.org/document/6196391>

Integration of high-level synthesis to the courses on reconfigurable digital systems

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander; Kruus, Margus** 2015 38th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO) : May 25-29, 2015, Opatija, Croatia : proceedings 2015 / p. 166-171 : ill <http://dx.doi.org/10.1109/MIPRO.2015.7160258>

Interactions of Zynq-7000 devices with general purpose computers through PCI-express : a case study [Electronic resource]

Rjabov, Artjom; Sudnitsõn, Aleksander; Sklyarov, Valery; Skliarova, Iuliia Proceedings of the 18th Mediterranean

Methodology and international collaboration in teaching reconfigurable systems

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** The 2012 IEEE Global Engineering Education Conference (IEEE EDUCON 2012), Marrakesh, Morocco, Apr. 17-20, 2012 / p. 1143-1152 : ill
https://www.researchgate.net/publication/254034783_Methodology_and_international_collaboration_in_teaching_reconfigurable_systems

Multilevel models for data processing

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE GCC Conference and Exhibition (GCC) : February 19-22, 2011, Dubai, United Arab Emirates 2011 / p. 136-139

Network-based hardware accelerators for parallel data processing = Võrgupõhised riistvarakiirendid paralleelseks andmetöötluseks

Rjabov, Artjom 2017 <https://digi.lib.ttu.ee/i/?8436> https://www.ester.ee/record=b4685402*est

Optimization of address-based data sorting unit with external memory support

Mihhailov, Dmitri; Rjabov, Artjom; Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander CompSysTech'13 : proceedings of the 14th International Conference on Computer Systems and Technologies 2013 / p. 83-90 : ill <https://doi.org/10.1145/2516775.2516807>
[Conference Proceedings at Scopus](#) [Article at Scopus](#)

Optimization of FPGA-based circuits for recursive data sorting

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 129-132 : ill

Optimization of recursive sorting algorithms for implementation in hardware

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander Proceedings of 22nd International Conference on Microelectronics (ICM 2010) : Cairo, Egypt, Dec. 19-22, 2010 / p. 471-474 : ill
https://www.researchgate.net/publication/224213497_Optimization_of_recursive_sorting_algorithms_for_implementation_in_hardware

Parallel FPGA-based implementation of recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 / p. 121-126 : ill
https://www.researchgate.net/publication/221437230_Parallel_FPGA-Based_Implementation_of_Recursive_Sorting_Algorithms

Parallel processing in FPGA-based digital circuits and systems

Sklyarov, Valery; Skliarova, Iuliia 2013 http://www.ester.ee/record=b2946103*est

Performance evaluation for FPGA-based processing of tree-like structures

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 19th IEEE International Conference on Electronics, Circuits, and Systems (IEEE ICECS), Sevilla, Spain, December 9-12, 2012 / p. 217-220 : ill
<https://ieeexplore.ieee.org/document/6463762>

Processing N-ary trees in hardware circuits

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 13th International Symposium on Integrated Circuits (ISIC) : Singapore, 12-14 December 2011 : proceedings 2011 / p. 262-265 : ill <https://ieeexplore.ieee.org/document/6131946>

Processing N-ary trees in reconfigurable hardware

Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander 2013 25th International Conference on Microelectronics (ICM) : 15-18 December 2013, Beirut-Lebanon 2013 / p. 13-16 : ill

Processing sorted subsets in a multi-level reconfigurable computing system

Rjabov, Artjom; Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander Elektronika ir elektrotehnika = Electronics and electrical engineering 2015 / p. 30-33 : ill <https://doi.org/10.5755/j01.eee.21.2.11509> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Processing tree-like data structures for sorting and managing priorities

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE Symposium on Computers & Informatics : ISCI 2011 : Kuala Lumpur, Malaysia, 20-23 March 2011 / p. 322-327
https://www.researchgate.net/publication/252020117_Processing_tree-like_data_structures_for_sorting_and_managing_priorities

Processing tree-like data structures in different computing platforms

Sklyarov, Valery; Skliarova, Iuliia; Oliveira, Ramiro; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 International Conference on Information and Computer Applications (ICICA 2011) : Dubai, United Arab Emirates, March 18-20, 2011 / p. 112-116 : ill
https://sweet.ua.pt/iouliia/Papers/2011/rp025_ICICA2011-A067.pdf

RAM-based mergers for data sort and frequent item computation [Electronic resource]

Rjabov, Artjom; Sklyarov, Valery; Skliarova, Ioulia; **Sudnitsõn, Aleksander** 2017 40th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO), May 22 - 26, 2017, Opatija, Croatia : proceedings 2017 / p. 176-181 : ill. [CD-ROM] <http://dx.doi.org/10.23919/MIPRO.2017.7973413>

Reconfigurable systems in engineering education : best practices and future trends

Skliarova, Ioulia; Sklyarov, Valery; **Sudnitsõn, Aleksander; Kruus, Margus** Proceedings of 2017 IEEE Global Engineering Education Conference (EDUCON) : 25-28 April 2017, Athens, Greece 2017 / p. 1084-1088 : ill
<https://doi.org/10.1109/EDUCON.2017.7942983>

Recursion and hierarchy in digital design and prototyping : a case study

Mihhailov, Dmitri; Kruus, Margus; Sklyarov, Valery; Skliarova, Ioulia; **Sudnitsõn, Aleksander** Computer Systems and Technologies : 12th International Conference, CompSysTech'11 : Vienna, Austria, June 16-17, 2011 : proceedings 2011 / p. 45-50 : ill
<https://dl.acm.org/doi/pdf/10.1145/2023607.2023616>

Solving computationally intensive problems in reconfigurable hardware : a case study

Skliarova, Ioulia; Vallejo, Tiago; Sklyarov, Valery; **Sudnitsõn, Aleksander; Kruus, Margus** Journal of convergence information technology (JCIT) : an international journal 2013 / p. 601-609 : ill

Synthesis and implementation of hierarchical finite state machines with implicit modules

Sklyarov, Valery; Skliarova, Ioulia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 2010 / p. 436-441 : ill
https://www.researchgate.net/publication/221437255_Synthesis_and_Implementation_of_Hierarchical_Finite_State_Machines_with_Implicit_Modules

Zynq-based system for extracting sorted subsets from large data sets

Sklyarov, Valery; Skliarova, Ioulia; **Rjabov, Artjom; Sudnitsõn, Aleksander** Journal of microelectronics, electronic components and materials 2015 / p. 142-152 : ill <https://ojs.midem-drustvo.si/index.php/InfMIDEM/article/view/117/0> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Teaching FPGA-based systems

Skliarova, Ioulia; Sklyarov, Valery; **Sudnitsõn, Aleksander; Kruus, Margus** 2014 IEEE Global Engineering Education Conference (EDUCON) : Istanbul, Turkey, April 2-5, 2014 2014 / p. 460-469 : ill

Using mobile technology to enhance teaching reconfigurable systems

Skliarova, Ioulia; Sklyarov, Valery; **Sudnitsõn, Aleksander; Kruus, Margus** Proceedings of 2013 IEEE International Conference on Teaching, Assessment and Learning for Engineering (TALE) 2013 / p. 478-483 : ill