Altera Niose ja Xilinx MicroBlaze'i võrdlus
Tagel, Mihkel A & A 2005 / 1, lk. 20-28

Alternatiivsete graafide mudel loogikalülituste funktsioonide kirjeldamiseks ja analüüsiks
Anton, E.; **Ubar, Raimund-Johannes** XXIX vabariiklik üliõpilaste teaduslik- tehniline konverents 30. märtsist - 1. aprillini 1977 : ettekannete teesid 1977 / lk. 42-43 https://www.ester.ee/record=b2449987*est

Another side of categorical propositions : the Keynes-Johnson octagon of oppositions
Moktefi, Amirouche; Schang, Fabien History and philosophy of logic 2023 / p. 459-475 https://doi.org/10.1080/01445340.2022.2143711 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Applying e-environments in teaching the basics of digital logic
Robal, Tarmo; **Kalja, Ahto** Proceedings MSE 2007 : 2007 IEEE International Conference on Microelectronic Systems Education : 3-4 June 2007, San Diego, CA 2007 / p. 41-42 : ill https://ieeexplore.ieee.org/document/4231440/keywords#keywords

At-speed testing and test quality evaluation for high-performance pipelined systems Töökiirusel testimine ja testi kvaliteedi hindamine kõrgjõudlus-konveierarhitektuuriga süsteemidele
Gorev, Maksim 2015 https://digi.lib.ttu.ee/i/?3953

Aufstellung von Testfolgen für logische Schaltungen
Plakk, Mari; **Ubar, Raimund-Johannes** Internationales wissenschaftliches Kolloquium 1979 / S. 93-96
https://www.ester.ee/record=b2936968*est

Boole'i algebra kasutamine automaatikalülituste projekteerimisel : loengukonspekt
Agur, Ustus 1972 https://www.ester.ee/record=b1327567*est

Clock manipulation for heterogeneous emulation environment
Ellervee, Peeter; Arhipov, Anton; **Tammemäe, Kalle** Proceedings [of] 24th IEEE Norchip Conference : Linköping, Sweden, 20-21 November 2006 2006 / p. 213-216 : ill https://ieeexplore.ieee.org/abstract/document/4126984

Computational kernel extraction for synthesis of power-managed sequential components
Sudnitsõn, Aleksander Proceedings of the 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS'2002, Dubrovnik, Croatia 2002 / p. 749-752 https://ieeexplore.ieee.org/abstract/document/1046277

Design of FPGA-based circuits using hierarchical finite state machines
Skliarova, Iouliia; Sklyarov, Valery; **Sudnitsõn, Aleksander** 2012 http://www.ester.ee/record=b2857138*est

Design of logical control devices
Zakrevskij, Arkadij; Pottosin, Yu.; Cheremisinova, L. 2009 https://www.ester.ee/record=b2548174*est

Digitaalarvutite loogikaelemendid ja trigerid : õppeabimaterjal
Mägi, Harri 1977 https://www.ester.ee/record=b1265883*est

Digitaalarvutite operatsioonelemendid ja aritmeetikaseadmed : õppevahend
Mägi, Harri 1978 https://www.ester.ee/record=b1274927*est

Digitaalarvutite operatsioonseadmed : õppevahend
Ubar, Raimund-Johannes 1978 https://www.ester.ee/record=b1313974*est

Distantskaitse loogikaosa
Allika, M.; **Simpson, V.** XXIX vabariiklik üliõpilaste teaduslik- tehniline konverents 30. märtsist - 1. aprillini 1977 : ettekannete teesid 1977 / lk. 69 https://www.ester.ee/record=b2449987*est

E-learning of digital logic
Robal, Tarmo; **Brik, Marina**; **Aarna, Margit** EWME 2006 proceedings : 6th International Workshop on Microelectronics Education : 8-9 June, 2006, Stockholm, Sweden 2006 / p. 120-123 : ill

Field-programmable logic and applications : from FPGAs to computing paradigm : 8th International Workshop, FPL'98, Tallinn, Estonia, August 31-September 3, 1998 : proceedings
Hartenstein, Reiner W.; **Keevallik, Andres** 1998 https://www.ester.ee/record=b1435446*est

Finite state machine synthesis for low power using input-disabling precomputation architectures
Sudnitsõn, Aleksander The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 137-140 : ill

FPGA implementation of the polynomial curve fitting
Gorev, Maksim; **Pesonen, Vadim** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 121-124 : ill

FPGA-based implementation of EEG analyzer
Gorev, Maksim; **Pesonen, Vadim**; **Mihhailov, Dmitri**; **Jenihhin, Maksim**; **Ellervee, Peeter** DATE'11 Friday Workshop on "Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing" : Grenoble, France, March 2011 2011 / [1] p
https://www.microsoft.com/en-us/research/wp-content/uploads/2017/03/ellervee.pdf

FPGA-based systems in information and communication
Sklyarov, Valery; Skliarova, Iouliia; **Sudnitsõn, Aleksander** AICT2011 : 5th International Conference on Application of Information and Communication Technologies : 12-14 October, Baku, Azerbaijan : conference proceedings 2011 / p. 551-555
https://www.researchgate.net/publication/254014990_FPGA-based_systems_in_information_and_communication

Hardware implementation of recursive sorting algorithms using tree-like structures and HFSM models = Rekursiivsete sortimisalgoritmide riistvaraline realiseerimine kasutades puulaadseid struktuure ja HFSM mudeleid
Mihhailov, Dmitri 2011 https://www.ester.ee/record=b2748823*est

High-speed logic level fault simulation
Ubar, Raimund-Johannes; **Devadze, Sergei** Design and test technology for dependable systems-on-chip 2011 / p. 310-335 : ill
https://www.igi-global.com/chapter/high-speed-logic-level-fault/51407

Hybrid protection of digital FIR filters
Aksoy, Levent; Nguyen, Quang-Linh; **Almeida, Felipe**; **Raik, Jaan**; Flottes, Marie-Lise; Dupuis, Sophie; **Pagliarini, Samuel Nascimento** IEEE transactions on Very Large Scale Integration (VLSI) Systems 2023 / p. 812-825 : ill
https://doi.org/10.1109/TVLSI.2023.3253641 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits
Jenihhin, Maksim; Squillero, Giovanni; **Tihhomirov, Valentin**; **Kostin, Sergei**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill https://doi.org/10.1007/s10836-016-5589-x Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Identification and rejuvenation of NBTI-critical paths in nanoscale logic circuits
Jenihhin, Maksim 1st International Workshop on Reliability and Aging in Forthcoming Electronic Systems : May 28-29, 2015, Cluj-Napoca, Romania 2015 / [1] p

Impulss-seadmed : laboratoorne töö nr. 5 : trigerid loogikaelementidel
1986 https://www.ester.ee/record=b1240931*est

Impulss-seadmed : laboratoorne töö nr. 8 : lineaarpinge generaator
1986 https://www.ester.ee/record=b2618544*est

Integraalsed loogikalülitused : katsestendi kirjeldus ja laboratoorsete tööde juhendid eriala "Elektriajamid ja tööstusseadmete automatiseerimine" 0628 üliõpilastele
1989 https://www.ester.ee/record=b1216651*est

Logic and system design of digital systems
Baranov, Samary; **Keevallik, Andres** 2008 https://www.ester.ee/record=b2358322*est

Loogikalülituste koostamise metoodika : õppevahend
Ariste, Andri 1978 https://www.ester.ee/record=b1305228*est

Loogikaskeemid ja binaardiagrammid
Buldas, Ahto Aastaraamat 1994 - 1996 / Eesti Matemaatika Selts 1999 / lk. 6-11

Model synthesis from VHDL for the functional test generation system
Krupnova, Helena 1993 https://www.ester.ee/record=b2090509*est

Modeling and simulation of circuits with shared structurally synthesized BDDs
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Raik, Jaan**; **Viies, Vladimir** Microprocessors and microsystems 2017 / p. 56-61 : ill
https://doi.org/10.1016/j.micpro.2016.09.006 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

On multiple fault detection in combinational logic circuits
Birger, Alexander BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 225-228

On pattern-based database design and implementation
Eessaar, Erki Proceedings : 6th ACIS International Conference on Software Engineering Research, Management and Applications : SERA 2008 : 20-22 August 2008, Prague, Czech Republic 2008 / p. 235-242
https://www.researchgate.net/publication/4370312_On_Pattern-Based_Database_Design_and_Implementation

Open source on-chip logic analyzer for FPGA-s
Ehrenpreis, Lauri; **Ellervee, Peeter**; **Tammemäe, Kalle** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 99-102 : ill

Operatsioonautomaadid digitaalarvutites : metoodiline materjal
1987 https://www.ester.ee/record=b1234461*est

Parallel processing in FPGA-based digital circuits and systems
Sklyarov, Valery; Skliarova, Iouliia 2013 http://www.ester.ee/record=b2946103*est

Performance evaluation for FPGA-based processing of tree-like structures
Sklyarov, Valery; Skliarova, Iouliia; **Mihhailov, Dmitri**; **Sudnitsõn, Aleksander** 19th IEEE International Conference on Electronics, Circuits, and Systems (IEEE ICECS), Sevilla, Spain, December 9-12, 2012 2012 / p. 217-220 : ill
https://ieeexplore.ieee.org/document/6463762

Programmeeritavad loogikaelemendid
Roasto, Indrek Elektriala 2006 / 1, lk. 24-26 : ill

Recursion and hierarchy in digital design and prototyping : a case study
Mihhailov, Dmitri; **Kruus, Margus**; Sklyarov, Valery; Skliarova, Iouliia; **Sudnitsõn, Aleksander** Computer Systems and Technologies : 12th International Conference, CompSysTech'11 : Vienna, Austria, June 16-17, 2011 : proceedings 2011 / p. 45-50 : ill
https://dl.acm.org/doi/pdf/10.1145/2023607.2023616

RESAA: A Removal and Structural Analysis Attack Against Compound Logic Locking
Almeida, Felipe; **Aksoy, Levent**; **Pagliarini, Samuel Nascimento** IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2025 / p. 1348-1360 https://doi.org//10.1109/TVLSI.2025.3534658

RESAA: A Removal and Structural Analysis Attack Against Compound Logic Locking : [preprint]
Almeida, Felipe; **Aksoy, Levent**; **Pagliarini, Samuel Nascimento** arXiv.org 2025 / 12 p. : ill https://doi.org/10.48550/arXiv.2409.16959

Resynthesis-based attacks against logic locking
Almeida, Felipe; **Aksoy, Levent**; Nguyen, Quang-Linh; Dupuis, Sophie; Flottes, Marie-Lise; **Pagliarini, Samuel Nascimento** 2023 24th International Symposium on Quality Electronic Design (ISQED) : San Francisco, 5-7 April 2023 2023 / 8 p. : ill
https://doi.org/10.1109/ISQED57927.2023.10129403 Article at Scopus Article at WOS

Shift register based TPG for at-speed interconnect BIST
Jutman, Artur MIEL 2004 : 24th International Conference on Microelectronics : Niš, Serbia and Montenegro, 16-19 May 2004 : proceedings. Volume 2 2004 / p. 751-754 : ill https://ieeexplore.ieee.org/document/1314941?signout=success

3D parallel fault simulation
Gorev, Maksim; **Ubar, Raimund-Johannes** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 39-42 : ill

Translating behavioral VHDL for emulation
Ellervee, Peeter; **Reinsalu, Uljana**; **Arhipov, Anton** 25th IEEE NORCHIP Conference : Aalborg, Denmark, 19-20 November 2007 2007 / ? p https://ieeexplore.ieee.org/document/4481073

Алгоритм генерирования тестов для комбинационных логических схем
Pall, I.; **Ubar, Raimund-Johannes** XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с. 133 https://www.ester.ee/record=b1306141*est

Декомпозиционный метод диагноза неисправностей в комбинационных схемах
Ubar, Raimund-Johannes Анализ и моделирование технических устройств и систем АСУТП 1978 / с. 3-22 : илл
https://www.ester.ee/record=b2191003*est https://digikogu.taltech.ee/et/Item/00fbff38-ccfb-411c-ad55-0c6b943b766b

Импульсные устройства : лабораторная работа No 5 : триггеры на логических элементах
1988 https://www.ester.ee/record=b1224918*est

Метод дедуктивного анализа тестов для логических схем
Viilup, Agu; **Kitsnik, Peeter**; **Ubar, Raimund-Johannes** Вопросы технической диагностики 1977 / с. [?]

https://www.ester.ee/record=b2353473*est

Метод сжатия диагностических словарей для логических схем
Suga, M.; **Ubar, Raimund-Johannes** XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с.135-136 https://www.ester.ee/record=b1306141*est

О синтезе логических схем : автореферат ... кандидата физико-математических наук
Hanko, Piia 1965 https://www.ester.ee/record=b1358931*est

О синтезе логических схем : диссертация на соискание ученой степени физико-математических наук
Hanko, Piia 1964

Параллельное интерпретативное моделирование тестов для комбинационных логических схем
Puntso, T.; **Ubar, Raimund-Johannes** XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с. 134 https://www.ester.ee/record=b1306141*est

Применение алгебры Буля при проектировании схем автоматики : конспект лекций
Agur, Ustus 1974 https://www.ester.ee/record=b1292481*est

Разработка и исследование оптимизационных методов декомпозиционного синтеза управляющих автоматов в базисе программируемых логических устройств : автореферат ... кандидата технических наук (05.13.01)
Berkman, Boriss 1989 https://www.ester.ee/record=b1225548*est

Разработка и исследование оптимизационных методов декомпозиционного синтеза управляющих автоматов в базисе программируемых логических устройств : диссертация на соискание ученой степени кандидата технических наук
Berkman, Boriss 1989 https://www.ester.ee/record=b4636210*est

Система управления инвертором на диодтранзисторных логических элементах
Irs, Rein; **Pikkov, Otto**; **Šilf, K.**; **Tomson, Jaan**; Šadeiko, T. Электромеханика. 3 1970 / с. 23-27 : илл
https://www.ester.ee/record=b2189951*est https://digikogu.taltech.ee/et/Item/ba0097d6-af8f-4557-96a1-ac545e315074/

Управление процессами диагноза логических схем
Toome, T.; **Ubar, Raimund-Johannes**; **Evartson, Teet** Тезисы докладов XXXI студенческой научно-технической конференции 1980 / с. 55-57 https://www.ester.ee/record=b1319482*est