

AC measurement converters : analog and digital solutions

Märtens, Olev 2000 http://www.ester.ee/record=b1707866*est

AG-model for design of testable controllers

Kasirova, Lilia BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 303-306: ill

Algorithms for hierarchical fault simulation in digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Klüver, B. Proceedings of the 10th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2003 : Lodz, Poland, 26-28 June 2003 2003 / p. 530-535 : ill

Alternative graph based test design in digital systems

Ubar, Raimund-Johannes Proceedings of 11. NORCHIP seminar, Trondheim, Nov. 9-10, 1993 1993 / p. 48-62

Alternative graphs and test pattern design in digital systems

Ubar, Raimund-Johannes Proc. of the 6th Workshop on New Directions for Testing, Montreal, Canada, May 20-22, 1992 1992

Alternative graphs as a mathematical tool and knowledge representation for diagnosis purposes in digital systems

Ubar, Raimund-Johannes BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 285-292: ill

An educational environment for digital testing : hardware, tools, and web-based runtime platform

Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes; Vislogubov, Vladislav Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 412-419 : ill https://www.researchgate.net/profile/Artur-Jutman/publication/220880167_An_Educational_Environment_for_Digital_Testing_Hardware_Tools_and_Web-Based_Runtime_Platform/links/02e7e53c3c71b0b2a7000000/An-Educational-Environment-for-Digital-Testing-Hardware-Tools-and-Web-Based-Runtime-Platform.pdf

Applying FPGA partial reconfiguration for digital system simulation

Arhipov, Anton; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 145-148 : ill

Asynchronous e-learning resources for hardware design issues

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of the International Conference on Computer Systems and Technologies (e-learning) : CompSysTech'04 : Rousse, Bulgaria, 17-18 June 2004 / p. IV.11-1 - IV.11-6 : ill https://www.researchgate.net/publication/234797327_Asynchronous_e-learning_resources_for_hardware_design_issues

At-speed on-chip diagnosis of board-level interconnect faults

Jutman, Artur Ninth IEEE European Test Symposium : ETS 2004 : 23-26 May 2004, Corsica, France : proceedings 2004 / p. 2-7 : ill https://www.researchgate.net/publication/4098807_At-speed_on-chip_diagnosis_of_board-level_interconnect_faults

At-speed testing and test quality evaluation for high-performance pipelined systems Töökiirusel testimine ja testi kvaliteedi hindamine kõrgjõudlus-konveierarhitektuuriga süsteemidele

Gorev, Maksim 2015 <https://digi.lib.ttu.ee//?3953>

Automated correction of design errors by edge redirection on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan 13th International Symposium on Quality Electronic Design (ISQED), 2012 2012 / p. 686-693 : ill <https://ieeexplore.ieee.org/document/6113980>

Automated test bench generation for high-level synthesis flow ABELITE

Viilukas, Taavi; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Baranov, Samary Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2011) : Sevastopol, Ukraine, September 9-12, 2011 2011 / p. 13-16 : ill <https://ieeexplore.ieee.org/document/6116601>

Back-traced deductive-parallel fault simulation for digital systems

Hahanov, Vladimir; Ubar, Raimund-Johannes; Hyduke, Stanley Proceedings : Euromicro Symposium on Digital System Design : Belek-Antalya, Turkey, September 1st to 6th, 2003 2003 / p. 370-377 : ill <https://ieeexplore.ieee.org/document/1231969>

Behavioral level modeling of digital systems for testing purposes

Ubar, Raimund-Johannes 42nd International Conference, Ilmenau, Germany, September 22-25, 1997. Part 1 1997 / p. 510-515

Berechnung von tests für die Fehlerdiagnose in Digitalsystem

Ubar, Raimund-Johannes Internationales wissenschaftliches Kolloquium, 21. 1. November bis 5. November 1976, H. 2: Vortragsreihe A 2: Entwurf, Analyse und Einsatz von informationsverarbeitenden Systemen: IWK 1976 / p. [?]

Bringing research issues into lab scenarios on the example of SoC testing [Electronic resource]

Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei; Wuttke, Heinz-Dietrich International Conference on Engineering Education - ICEE 2007 : September 3-7, 2007, Coimbra, Portugal 2007 / [7] p. : ill. [CD-ROM]
<http://icee2007.dei.uc.pt/proceedings/papers/429.pdf>

Built-in self diagnosis with multiple signature analyzers in digital systems

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 29-34 : ill

CAD für Digitaltechnik - eine Programmfamilie für den Entwurf von Testmustern zum Test von Digitalschaltungen

Ubar, Raimund-Johannes IBM Hochschulkongress '92: Offene Grenzen - offene Systeme, Dresden, 30.09-2.10.1992 1992 / S.IV/9 1-14

Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Microprocessors and microsystems 2020 / art. 103117, 12 p <https://doi.org/10.1016/j.micpro.2020.103117> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Combining functional and structural approaches in test generation for digital systems

Ubar, Raimund-Johannes Microelectronics reliability 1998 / 3, p. 317-329 : ill

Comparison of two approaches to improve functional BIST fault coverage

Kostin, Sergei; Ubar, Raimund-Johannes; Gorev, Maksim; Mägi, Gunnar BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 105-108 : ill

Conditional fault collapsing in digital circuits with shared structurally synthesized BDDs [Online resource]

Jürimägi, Lembit; Ubar, Raimund-Johannes BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p. : ill <https://doi.org/10.1109/BEC.2018.8600967>

A constraint-driven gate-level test generator

Raik, Jaan; Ubar, Raimund-Johannes; Jervan, Gert; Krupnova, Helena BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 237-240: ill

Constraints analysis in hierarchical test generation for digital systems

Ubar, Raimund-Johannes; Krupnova, Helena BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 313-318: ill

Cycle-based simulation with decision diagrams

Ubar, Raimund-Johannes; Morawiec, Adam; Raik, Jaan Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 454-458: ill <https://ieeexplore.ieee.org/document/761165>

A decision diagram based hierarchical test pattern generator

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 159-162: ill

Decision diagrams - from a mathematical notion to engineering applications

Stankovic, Radomir S.; **Ubar, Raimund-Johannes;** Astola, Jaakko Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 281-301 : ill <http://dx.doi.org/10.2298/FUEE1103281S>

Decision diagrams and digital test

Ubar, Raimund-Johannes ECMS 2003 : 6th International Workshop on Electronics, Control, Measurement and Signals : Liberec, Czechia, June 2-4, 2003 2003 / p. 266-273 : ill [http://www.midem-drustvo.si/Journal%20papers/MIDEM_35\(2005\)4p187.pdf](http://www.midem-drustvo.si/Journal%20papers/MIDEM_35(2005)4p187.pdf)

Deductive fault simulation on structurally synthesized BDDs

Aarna, Margit; Ubar, Raimund-Johannes; Raik, Jaan BEC 2004 : Baltic Electronics Conference : Post-Graduate Student Session : Tallinn University of Technology, October 3-6, 2004, Tallinn, Estonia 2004 / p. 11 : ill

Defect-oriented fault simulation and test generation in digital circuits

Kuzmich, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE ISQED 2001 : proceedings of the IEEE 2001 2nd International Symposium on Quality Electronic Design : March 26-28, 2001, San Jose, California 2001 / p. 365-371
<https://ieeexplore.ieee.org/document/915257>

Defect-oriented mixed-level fault simulation in digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Briik, Marina Facta Universitatis [Niš]. Series electronics and energetics 2002 / 1, April, p. 123-136 : ill

Defect-oriented test generation and fault simulation in the environment of MOSCITO

Schneider, Andre; Diener, Karl-Heinz; Gramatova, Elena; Fisherova, Maria; **Ivask, Eero; Ubar, Raimund-Johannes**; Pleskacz, Witold A.; Kuzmicz, W. BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 303-306 : ill

Design and verification of Cyber-Physical Systems using TrueTime, evolutionary optimization and UPPAAL

Balasubramaniyan, Sreram; Srinivasan, Seshadhri; Buonopane, Furio; Balasubramanian, Subathra; **Vain, Jüri**; Ramaswamy, Srin Microprocessors and microsystems 2016 / p. 37-48 : ill <https://doi.org/10.1016/j.micpro.2015.12.006> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Design error diagnosis in digital circuits without error model

Ubar, Raimund-Johannes; Borriore, Dominique VLSI : systems on a chip : IFIP TC10 WG10.5 Tenth International Conference on Very Large Scale Integration (VLSI'99) : December 1-4, 1999, Lisboa, Portugal 1999 / p. 281-292 : ill https://www.researchgate.net/publication/292157544_Design_Error_Diagnosis_in_Digital_Circuits_without_Error_Model

Design error diagnosis using backtrace algorithm on decision diagrams

Repinski, Urmas; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

Diagnostic modeling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill https://www.researchgate.net/publication/344994231_Diagnostic_Modeling_of_Digital_Systems_with_Multi-Level_Decision_Diagrams

Diagnostic modelling of digital systems with binary and high-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Kruus, Helena; Lensen, Harri; Evertson, Teet Progress in industrial mathematics at ECMI 2006 2008 / p. 902-907 : ill https://link.springer.com/chapter/10.1007/978-3-540-71992-2_158

Diagnostic modelling of digital systems with decision diagrams

Ubar, Raimund-Johannes Вестник Томского государственного университета : приложение 2004 / август, материалы международных, всесоюзных и региональных научных конференций, симпозиумов, школ, проводимых в ТГУ, с. 174-179 : ил

Diagnostic modelling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Evertson, Teet; Kruus, Margus; Lensen, Harri Proceedings of the 17th IASTED International Conference on Modelling and Simulation : May 24-26, 2006, Montreal, Quebec, Canada 2006 / p. 207-212 : ill

Digievolutsiooni võimalused koolihariduses

Jürjo, Silvester Studioosus 2015 / lk. 20-21 https://www.ester.ee/record=b1558644*est

Digitaalseadmete simuleerimine : õppemetoodiline vahend

1989 https://www.ester.ee/record=b1221053*est

Digitaalseadmete struktuuri projekteerimine : õppevahend

Ariste, Andri 1978 https://www.ester.ee/record=b1305228*est

Digitaalsüsteemide diagnostika

Ubar, Raimund-Johannes 2005 http://www.ester.ee/record=b2097071*est

Digitaalsüsteemide diagnostika Tallinna Tehnikaülikoolis

Ubar, Raimund-Johannes Teadusmõtte Eestis : tehnikateadused 2002 / lk. 107-113 : ill

Digitaaltehnika doktorantidele. Osa II, Kombinatsioon- ja järjendlülitused = Digital engineering. Part II, Combinational and sequential circuits [Võrguväljaanne]

Lehtla, Madis 2014 http://egdk.ttu.ee/files/2014/Digitaaltehnika_doktorantidele2.pdf

Digitaaltelevisiorid

Schults, Eduard Side. Raadio. Televisioon : infoseeria 10 1984 / lk. 8-10 : ill https://www.ester.ee/record=b1232303~S1*est

Digital design at microarch[itectural] level based on quality relationship measures

Kruus, Margus; Lensen, Harri; Sudnitsõn, Aleksander Успехи современного естествознания 2004 / 5, приложение 1, Материалы XXXI международной конференции и дискуссионного научного клуба : информационные технологии в науке, образовании, телекоммуникации и бизнесе : IT+SE'2004 : Украина, Крым, Ялта-Гурзуф, 18-27 мая 2004 года, с. 29-30

Digital electronics design and test at Computer Engineering Department of Tallinn University of Technology

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Ellervee, Peeter The house magazine : the parliamentary weekly 2006 / 1198, p. 42 : ill

Digital hardware organization course for SoC program

Ellervee, Peeter; Tenhunen, Hannu 2001 International Conference on Microelectronic Systems Education : June 17-18, 2001, Las Vegas, Nevada, USA : proceedings 2001 / p. 26-27 <https://ieeexplore.ieee.org/document/932402>

Digital last planner system whiteboard for enabling remote collaborative design process planning and control

Pikas, Ergo; Pedo, Barbara; Tezel, Algan; Koskela, Lauri; **Veersoo, Markus** Sustainability 2022 / art. 12030
<https://doi.org/10.3390/su141912030> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

A digital measuring module for tool wear estimation

Otto, Tauno; Kurik, Lembit; Papstel, Jüri DAAAM international scientific book 2003 2003 / p. 435-444

Digital object memory based monitoring and assistance applications in manual work station

Aruväli, Tanel 14th International Symposium "Topical problems in the field of electrical and power engineering. Doctoral school of energy and geotechnology. II" : Pärnu, Estonia, January 13-18, 2014 2014 / p. 274-276 : ill

Digital synthesis tools for education and research

Fomina, Jelena; Ellervee, Peeter; Kruus, Margus; Sudnitsõn, Aleksander; Tammemäe, Kalle Proc. 18th International Conference on Systems for Automation of Engineering and Research (SAER'2004) 2004 / p. 160-164

Digital techniques in magnetic measurements

Ripka, Pavel; Kašpar, Petr; Roztocil, Jaroslav; Platil, Antonin BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 153-154: ill

Distance-learning tools for digital design and test issues

Jutman, Artur; Kruus, Margus; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes IT+SE'2002 : Information Tec[h]nologies in Science, Education, Telecommunication, Business : proceedings = Информационные технологии в науке, образовании, телекоммуникации, бизнесе, Украина, Крым, Ялта-Гурзуф, 20-30 мая 2002 года : труды 2002 / p. 269-272 : ill

Double phase fault collapsing with linear complexity in digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Orasson, Elmet; Josifovska, Galina; Oyeniran, Adeboye Stephen DSD 2015 : 18th Euromicro Conference on Digital Systems Design : 26-28 August 2015, Funchal, Madeira, Portugal 2015 / p. 700-705 : ill

Effect of keysight 3458A jitter on precision of phase difference measurement

Pokatilov, Andrei; Kübarsepp, Toomas; Vabson, Viktor IEEE transactions on instrumentation and measurement 2016 / p. 2595-2600 : ill <https://doi.org/10.1109/TIM.2016.2593965> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

E-learning tool and excercises for teaching digital test

Ubar, Raimund-Johannes; Orasson, Elmet Proceedings of the 2nd IEEE Conference on Signals, Systems, Decision and Information Technology : Sousse, Tunisia, 2003 2003 / [6] p. : ill <https://pld.ttu.ee/dildis/publications/E-Learning%20tool%20and%20Exercises.pdf>

E-learning tools for digital test

Devadze, Sergei; Gorjachev, R.; **Jutman, Artur; Orasson, Elmet**; Rosin, Vjatšeslav; **Ubar, Raimund-Johannes** Proc. III International Conference "Distance Learning - Educational Sphere of XXI Century" : Minsk, Belorussia, 2003 2003 / p. 336-342

Embedded diagnosis in digital systems

Kostin, Sergei Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 81-84 : ill

Embedded diagnosis in digital systems

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan 2008 26th International Conference on Microelectronics : Niš, Serbia, 11-14 May 2008 : proceedings. Vol. 2 2008 / p. 421-424 : ill

Embedded fault diagnosis in digital systems with BIST

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan Microprocessors and microsystems 2008 / 5/6, p. 279-287 : ill

Environment for the analysis of functional self-test quality in digital systems

Ubar, Raimund-Johannes; Kostin, Sergei; Kruus, Helena; Aarna, Margit; Devadze, Sergei Proceedings of the Estonian Academy of Sciences 2014 / p. 151-162 : ill https://artiklid.elnet.ee/record=b2673964*est <https://doi.org/10.3176/proc.2014.2.05> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Equivalent transformations of structurally synthesized BDDs and applications

Jürimägi, Lembit; Ubar, Raimund-Johannes; Viies, Vladimir 2019 8th Mediterranean Conference on Embedded Computing

(MECO) 2019 / 6 p. : ill <https://doi.org/10.1109/MECO.2019.8760283>

Estonia huku uurimine jätkub, kuigi valitsus pole lisaraha veel eraldanud [Võrguväljaanne]

Linnart, Mart err.ee 2022 [Estonia huku uurimine jätkub, kuigi valitsus pole lisaraha veel eraldanud](#)

EUROCHIP - kursus digitaalsüsteemide kõrgtaseme sünteesist : [Leuven, Belgia : aug.-sept.]

Tammemäe, Kalle Arvutustehnika ja Andmetöötlus 1994 / 11, lk. 15-21

Evaluation of the latency components in MPEG-4 DVB-T system

Äniline, Janno Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuseum 2007 / lk. 77-80

Fast RTL fault simulation using decision diagrams and bitwise set operations

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes; Ellervee, Peeter 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 3-5 October 2011, Vancouver, Canada 2011 / p. 164-170
<https://ieeexplore.ieee.org/document/6104440>

Fault model and test synthesis for RISC-processors

Ubar, Raimund-Johannes; Markus, Antti; Jervan, Gert; Raik, Jaan BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 229-232: ill

Fault modeling and diagnosis in digital systems

Ubar, Raimund-Johannes CREDES Summer School : Dependable Systems Design : handouts 2011 / p. 91-106 : ill

Fault simulation and code coverage analysis of RTL designs using high-level decision diagrams = Rikete simuleerimine ja koodikatte analüüs register-siirde tasemel kasutades kõrgtaseme otsustusdiagramme

Reinsalu, Uljana 2013 https://www.ester.ee/record=b2963595*est

Fault simulation of digital systems = Digitaalsüsteemide rikete simuleerimine

Devadze, Sergei 2009 <https://digi.lib.ttu.ee/ii/?445> https://www.ester.ee/record=b2508727*est

Foreword to the 12th IEEE DDECS Symposium

Pliva, Zdenek; Manhaeve, Hans; Renovell, Michel; Novak, Ondrej; Ubar, Raimund-Johannes; Drabkova, Jindra Proceedings of the 2009 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 15-17, 2009, Liberec, Czech Republic 2009 / p. iii <http://dx.doi.org/10.1109/DDECS.2009.5012081>

Formal verification and error correction on high-level decision diagrams = Formaalne verifitseerimine ja vigade parandamine kõrgtasemelistel otsustusdiagrammidel

Karputkin, Anton 2012

FPGA based fault emulation of synchronous sequential circuits

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin; Ubar, Raimund-Johannes Proceedings [of] 22nd NORCHIP Conference : Oslo, Norway, 8-9 November 2004 2004 / p. 59-62 <https://ieeexplore.ieee.org/abstract/document/1423822>

Functional level test set generation methods

Ubar, Raimund-Johannes Proceedings of the 12th Conference on Fault-Tolerant Systems and Diagnostics, Prague, Czechoslovakia, September, 1989 1989 / p. 46-55

Functional self-test of high-performance pipe-lined signal processing architectures

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart Microprocessors and microsystems 2015 / p. 909-918 : ill <https://doi.org/10.1016/j.micpro.2014.11.002> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Functional specification and testing of digital systems

Ubar, Raimund-Johannes Multimicroprocessor systems: Proceedings of the 3rd Symposium, Stralsund, oct. 16-20, 1989, Vol 1 1989 / p. 207-217

Functional test program generation for digital systems

Ubar, Raimund-Johannes; Dušina, Julia; Krupnova, Helena; Storozhev, Sergei; Zaugarov, Viktor Testmethoden und Zuverlässigkeit von Schaltungen und Systemen : proceedings of the 6th workshop, Vaals (Niederlande), March 6-8, 1994 1994 / p. 14-18: ill

GA-based test generation for sequential circuits

Brik, Marina; Raik, Jaan; Ubar, Raimund-Johannes; Ivask, Eero Proceedings of East-West Design & Test Workshop (EWDWTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 30-34

A general approach to synthesis of the finite-state machine logical structure in the sum-of-products form

Chapenko, V.; Fritsnovich, G.; Kalnberzin, A.; Lange, E. BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 2 1994 / p. 385-390 https://www.estee.ee/record=b2150914*est

Genetic algorithm approach to the problem of finite state machine construction

Spitšakova, Margarita Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 69-72 : ill

Guide to the digital switchover

Nyman-Metcalf, Katrin Merike; Richter, Andrei 2010 <https://www.osce.org/files/f/documents/8/c/73720.pdf>

Hierarchical approach to test generation for digital systems at system, circuit and defect levels

Ubar, Raimund-Johannes 45. Internationales Wissenschaftliches Kolloquium, 04.-06.10.2000 : Tagungsband 2000 / S. 711-716 : ill

Hierarchical design error diagnosis in combinational circuits by stuck-at fault test patterns

Ubar, Raimund-Johannes; Jutman, Artur Proceedings of the 6th International Conference on Mixed Design of Integrated Circuits and Systems : MIXDES'99 : Krakow, Poland, 17-19 June 1999 1999 / p. 437-442 : ill
<https://www.sciencedirect.com/science/article/pii/S0026271499002036>

Hierarchical fault diagnosis in embedded digital systems with multi-level decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Evertson, Teet; Lensen, Harri; Aarna, Margit 5th International Conference on Industrial Automation = Cinquieme Conference Internationale sur l'Automatisation Industrielle : June 11-13, 2007, Montreal, Canada 2007 / [6] p. [CD-ROM]

Hierarchical fault simulation in digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina International Symposium on Signals, Circuits and Systems : SCS 2001 : July 10-11, 2001, Iasi, Romania : proceedings 2001 / p. 181-184 : ill

Hierarchical test generation for complex digital systems with control and data processing parts

Ubar, Raimund-Johannes; Raik, Jaan "Test, Assembly and Packaging" : SEMICON Technical Symposium : Singapur, May 3-6, 1999 1999 / p. 43-52

Hierarchical test generation for digital systems

Brik, Marina; Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Mixed design of integrated circuits and systems 1998 / p. 131-136: ill https://link.springer.com/chapter/10.1007/978-1-4615-5651-0_20

Hierarchical test generation for digital systems based on combining bottom-up and top-down approaches

Raik, Jaan; Ubar, Raimund-Johannes World Multiconference on Systemics, Cybernetics and Informatics, July 12-16, 1998, Orlando, Florida : proceedings. Vol. 1 1998 / p. 374-381: ill

Hierarchical test generation with multi-level decision diagram models

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 7th IEEE North Atlantic Test Workshop, West Greenwich RI, USA, May 28-29, 1998 1998 / p. 26-33
https://www.academia.edu/67811738/Hierarchical_Test_Generation_with_Multi_Level_Decision_Diagram_Models?hb-g-sw=7883185

Hierarchical test generation. SEMI show slides

Ubar, Raimund-Johannes; Raik, Jaan "Test, Assembly and Packaging" : SEMICON Technical Symposium : Singapur, May 3-6, 1999 1999 / p. 53-64

Hierarchical test synthesis for digital systems using alternative graph model

Ubar, Raimund-Johannes Quantitative aspects of designing and validating dependable computing systems 1995

High level fault modeling in digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Brik, Marina; Raik, Jaan Synergies between Information and Automation : 49. Internationales Wissenschaftliches Kolloquium, 27.-30.9.2004, Technische Universität Ilmenau, Germany. Volume 2 2004 / p. 486-491

High quality test generation for digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Kruus, Helena; Raik, Jaan Romanian journal of information science and technology 2005 / 1, p. 73-84 : ill

High-Level Decision Diagram manipulations for code coverage analysis

Minakova, Karina; Reinsalu, Uljana; Tšepurov, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level synthesis and test in the MOSCITO-based virtual laboratory

Schneider, Andre; Diener, Karl-Heinz; **Jervan, Gert**; Peng, Z.; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Hollstein, Thomas; Glesner, M. BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 287-290 : ill

How to generate high quality tests for digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Kruus, Helena; Raik, Jaan 2004 International Semiconductor Conference : 27th edition, October 4-6, 2004, Sinaia, Romania : CAS 2004 proceedings. Volume 2 2004 / p. 459-462 : ill
<http://dx.doi.org/10.1109/SMICND.2004.1403048>

Hybrid BIST optimization for core-based systems with test pattern broadcasting

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Zebo DELTA 2004 : second IEEE International Workshop on Electronic Design, Test and Applications : 28-30 January 2004, Perth, Australia : proceedings 2004 / p. 3-8 : ill
<https://ieeexplore.ieee.org/document/1409808>

Hybrid functional BIST for digital systems

Mazurova, Natalja; Smahtina, Julia; Ubar, Raimund-Johannes BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 205-208 : ill

HyFBIST : hybrid functional built-in self-test in microprogrammed data-paths of digital systems

Ubar, Raimund-Johannes; Mazurova, Natalja; Smahtina, Julia; Orasson, Elmet; Raik, Jaan Proceedings of the 11th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2004 : Szczecin, Poland, 24-26 June 2004 2004 / p. 497-502 : ill

Implementation of Digital Twins for electrical energy conversion systems in selected case studies

Rassõlkin, Anton; Orosz, Tamas; Demidova, Galina; Kuts, Vladimir; Rjabtšikov, Viktor; Vaimann, Toomas; Kallaste, Ants Proceedings of the Estonian Academy of Sciences 2021 / p. 19-39 : ill <https://doi.org/10.3176/proc.2021.1.03> https://doi.org/wp-content/plugins/kirj/pub/proc-1-2021-19-39_20210201183802.pdf Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

An improved estimation methodology for hybrid BIST cost calculation

Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes**; Korelina, Olga Proceedings [of] 22nd NORCHIP Conference : Oslo, Norway, 8-9 November 2004 2004 / p. 297-300 : ill <https://ieeexplore.ieee.org/document/1423882>

An improved estimation technique for hybrid BIST test set generation

Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes**; Korelina, Olga DDECS : 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 13-16, 2005, Sopron, Hungary : proceedings 2005 / p. 182-185 : ill
<https://www.ida.liu.se/labs/eslab/publications/pap/db/ddecs05.pdf>

Improved VHDL input for high-level synthesis tool xTractor

Ellervee, Peeter; Ivask, Eero; Kruus, Margus BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 87-90 : ill

Insener projekteerib usaldust : [ka TTÜ arvutitehnika instituudi töödest]

Ubar, Raimund-Johannes Arvutimaailm 2011 / 7/8, lk. 8-9 : ill https://artiklid.elnet.ee/record=b2423013*est

Integration of high-level synthesis to the courses on reconfigurable digital systems

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander; Kruus, Margus** 2015 38th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO) : May 25-29, 2015, Opatija, Croatia : proceedings 2015 / p. 166-171 : ill <http://dx.doi.org/10.1109/MIPRO.2015.7160258>

Internet-based collaborative test generation with MOSCITO [Electronic resource]

Schneider, Andre; **Ivask, Eero**; Miklos, P.; **Raik, Jaan**; Diener, Karl-Heinz; **Ubar, Raimund-Johannes**; Cibakova, Tatiana; Gramatova, Elena SIGDA publications on CD-ROM : DATE'02 : Design, Automation and Test in Europe, Paris, France, March 4-8, 2002 2002 / [6] p. [CD-ROM] https://www.cecs.uci.edu/~papers/date07/PAPERS/2002/DATE02/PDFFILES/02E_2.PDF

Internet-based software for teaching test of digital circuits

Ubar, Raimund-Johannes; Orasson, Elmet; Wuttke, Heinz-Dietrich 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 659-662 : ill <https://ieeexplore.ieee.org/document/1003344>

Internet-based software for teaching test of digital circuits

Ubar, Raimund-Johannes; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Evartson, Teet; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 4th European Workshop on Microelectronics Education : EWME 2002, Spain, May 23-24, 2002 2002 / p. 317-320 : ill <https://ieeexplore.ieee.org/document/1003344>

Java applet for self-learning of digital test issues [Electronic resource]

Ubar, Raimund-Johannes; Orasson, Elmet; Evartson, Teet 13th EAEEIE Annual Conference, 8th-10th April, 2002, York, England 2002 / [4] p. [CD-ROM]

Java applets support for an asynchronous-mode learning of digital design and test

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich ITHET 2003 proceedings : 4th International Conference on Information Technology Based Higher Education and Training : July 7-9, 2003, Marrakech, Morocco 2003 / p. 397-401 : ill <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=92f0b0e5011a2192d5a1b98baa751cb8cd2f7ff3>

Java technology based training system for teaching digital design and test

Devadze, Sergei; Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 283-286 : ill

Kiiruse mõõtmise mobiilne süsteem : aastal 2009 avaldatud tööde koopiade kogumik. 13

Laaneots, Rein 2009 https://www.ester.ee/record=b2641827*est

Kvaliteetsema digiõppe poole

Puust, Raido Postimees 2021 / Lk. 14 <https://dea.digar.ee/article/postimees/2021/05/13/12.10>

Laboratory course for training "Digital design and test"

Ubar, Raimund-Johannes; Tulit, Viljar; Buldas, Ahto; **Saarepera, Märt** Fourth EUROCHIP Workshop on VLSI Design Training, 29 September to 1 October 1993, Toledo : [proceedings] 1993 / p. 112-117: ill

Localization of single-gate design errors in combinational circuits by diagnostic information about stuck-at faults

Ubar, Raimund-Johannes; Borriane, Dominique Proceedings of the 2nd International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Szczyrk, Poland, September 2-4, 1998 1998 / p. 73-79
https://www.researchgate.net/publication/238687832_Localization_of_Single_Gate_Design_Errors_in_Combinational_Circuits_by_Diagnostic_Information_about_Stuck-at_Faults

Logic and system design of digital systems

Baranov, Samary; **Keevalik, Andres** 2008 https://www.ester.ee/record=b2358322*est

Mapping faults in hierarchical testing of digital systems

Ubar, Raimund-Johannes International Conference on Computer, Communication and Control Technologies CCCT'03 and the 9th International Conference on Information Systems, Analysis and Synthesis ISAS'03 : July 31 - August 1-2, Orlando, Florida, USA : proceedings. Volume I, Computing/Information Systems and Technologies 2003 / p. 14-19 : ill

Mehaanika ja tööstustehnika instituudis valmivad elumuutvad lahendused [Võrguväljaanne]

Alver, Anne-Mari Eesti Päevaleht 2022 / Lk. 10 [Mehaanika ja tööstustehnika instituudis valmivad elumuutvad lahendused](#)

Methods for improving the accuracy and efficiency of fault simulation in digital systems = Meetodid digitaalsüsteemide rikete simuleerimise täpsuse ja efektiivsuse tõstmiseks

Kõusaar, Jaak 2019 <https://digi.lib.ttu.ee/i/?11667>

Millest tekkisid parvlaeva Estonia augud? Laevaehituse insener : teeme esimesi katsearvutusi

Riik, Marvel ohtuleht.ee 2023 / Lk. 2 [Millest tekkisid parvlaeva Estonia augud? Laevaehituse insener: teeme esimesi katsearvutusi](#)

Mixed bottom-up/top-down hierarchical test generation for digital systems

Ubar, Raimund-Johannes Proceedings of the 9th European Workshop on Dependable Computing, Gdansk, Poland, May 14-16, 1998 1998 / p. 37-40

Mixed-level defect simulation in data-paths of digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 617-620 : ill <https://ieeexplore.ieee.org/document/1003333>

Mixed-level test generator for digital systems

Brik, Marina; Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 1997 / 4, p. 271-282 : ill

Model synthesis from VHDL for the functional test generation system

Krupnova, Helena 1993 https://www.ester.ee/record=b2090509*est

MS Estonia ferry investigation continues, no additional funds yet allocated [Online resources]

Linnart, Mart news.err.ee 2022 [MS Estonia ferry investigation continues, no additional funds yet allocated](#)

Multi-level fault simulation of digital systems on decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina The First IEEE International Workshop on Electronic Design, Test and Applications : DELTA 2002, 29-31 January 2002, Christchurch, New Zealand : proceedings 2002 / p. 86-91 : ill

Multi-level test generation and fault diagnosis in digital systems

Ubar, Raimund-Johannes 1992

Multi-level test generation for digital systems at system, circuit and defect levels

Ubar, Raimund-Johannes Proceedings of the 7th International Scientific Conference "Theory and Technique of Information Transmission, Reception and Processing" : Tuapse, October 1-4, 2001 2001 / p. 286-288

Multiple fault testing in systems-on-chip with high-level decision diagrams

Ubar, Raimund-Johannes; Oyeniran, Adeboye Stephen; Schölzel, Mario; Vierhaus, Heinrich Theodor Proceedings of 2015 10th International Design & Test Symposium (IDT) : Dead Sea, Jordan, 14-16 December 2015 2015 / p. 66-71 : ill
<http://dx.doi.org/10.1109/IDT.2015.7396738>

Multivalued simulation on AG-model of digital devices

Ubar, Raimund-Johannes; Voolaine, Andrus Proceedings of the 12th Conference on Fault-Tolerant Systems and Diagnostics, Prague, Czechoslovakia, September, 1989 1989 / p. 101-104

Mutation analysis for systemC designs at TLM

Guarnieri, Valerio; Bombieri, Nicola; Pravadelli, Graziano; Fummi, Franco; **Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes** 12th IEEE Latin American Test Workshop (LATW) : Porto de Galinhas, Brasil, 27-30 March 2011 2011 / [6] p
<https://ieeexplore.ieee.org/document/5985925>

Mutation-based verification and error correction in high-level designs = Mutatsioonidel põhinev verifitseerimine ja vigade parandamine kõrgtaseme skeemides

Hantson, Hanno 2015 https://www.ester.ee/record=b4518212*est

Mõtteid koostöö võimalikkusest Ida-Lääne piiril

Ubar, Raimund-Johannes; Kruus, Margus Mente et Manu 2003 / 20. okt., lk. 2 : portr https://artiklid.elnet.ee/record=b1415646*est

New method of testability calculation to guide RT-level test generation

Raik, Jaan; Nõmmeots, Tanel; Ubar, Raimund-Johannes 4th IEEE Latin-American Test Workshop : LATW2003 : Natal, Brazil, February 16-19, 2003 2003 / p. 46-51 : ill <https://link.springer.com/article/10.1007/s10836-005-5288-5>

On correction of the results of a ternary simulation and a preliminary estimation of the correction results

Matrosova, Anjela; Golubeva, O.; Oshlakova, T. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 183-186: ill

On multiple fault detection in combinational logic circuits

Birger, Alexander BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 225-228

Optimization of boundary scan tests using FPGA-based efficient scan architectures

Aleksejev, Igor; Devadze, Sergei; Jutman, Artur; Shibin, Konstantin Journal of electronic testing : theory and applications (JETTA) 2016 / p. 245-255 : ill <https://doi.org/10.1007/s10836-016-5588-y> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Optimization of memory-constrained hybrid BIST for testing core-based systems

Jervan, Gert; Kruus, Helena; Orasson, Elmet; Ubar, Raimund-Johannes Proceedings of the IEEE 2nd International Symposium on Industrial Embedded Systems : SIES'2007 : Lisbon, Portugal, 4-6 July 2007 2007 / p. 71-77
<https://ieeexplore.ieee.org/document/4297319>

Optimization of memory-constrained hybrid BIST for testing core-based systems

Jervan, Gert; Kruus, Helena; Orasson, Elmet; Ubar, Raimund-Johannes Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 133-136 : ill

Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems

Ubar, Raimund-Johannes Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 303-324 : ill
<http://dx.doi.org/10.2298/FUEE1103303U>

Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems

Ubar, Raimund-Johannes Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 1-10 : ill
<https://scindeks-clanci.ceon.rs/data/pdf/0353-3670/2011/0353-36701103303U.pdf>

Overview of e-learning environment for web-based study of testing and diagnostics of digital systems

Jutman, Artur; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 5th European Workshop on Microelectronics Education, held in Lausanne, Switzerland, April 15-16, 2004 2004 / p. 253-258 : ill
https://link.springer.com/chapter/10.1007/978-1-4020-2651-5_41

Overview of e-learning environment for web-based study of testing and diagnostics of digital systems

Jutman, Artur; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 5th European Workshop on Microelectronics Education - EWME 2004, Lausanne, 2004 / p. 173-176 https://link.springer.com/chapter/10.1007/978-1-4020-2651-5_41

Parallel critical path tracing fault simulation

Ubar, Raimund-Johannes 39. Internationales Wissenschaftliches Kolloquium : 27.-30.09.1994. Bd. 1, Vortragsreihen 1994 / S. 399-404

Parallel fault simulation in digital circuits

Aarna, Margit; **Raik, Jaan; Ubar, Raimund-Johannes** Scientific proceedings of Riga Technical University. 7. serija, Telecommunications and electronics 2001 / p. 91-94 : ill

Parallel fault simulation in digital circuits

Aarna, Margit; **Raik, Jaan; Ubar, Raimund-Johannes** Proc. of 42nd International Scientific Conference of Riga Technical University 2001 / p. 91-94

Power-constrained hybrid BIST test scheduling in an abort-on-first-fail test environment

He, Zhiyuan; **Jervan, Gert; Peng, Zebao; Eles, Petru** Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 / p. 83-86 : ill
<https://ieeexplore.ieee.org/document/1559782>

Probabilistic equivalence checking based on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 423-428 : ill
<https://ieeexplore.ieee.org/document/5783130>

PSL assertions based verification with HLDD tools

Jenihhin, Maksim Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 17-20 : ill

Register transfer low power design based on controller decomposition

Sudnitsõn, Aleksander MIEL 2004 : 24th International Conference on Microelectronics : Niš, Serbia and Montenegro, 16-19 May 2004 : proceedings. Volume 2 2004 / p. 735-738 : ill <https://ieeexplore.ieee.org/document/1314937>

Research environment for teaching digital test

Ivask, Eero; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Synergies between Information and Automation : 49. Internationales Wissenschaftliches Kolloquium, 27.-30.9.2004, Technische Universität Ilmenau, Germany. Volume 2 2004 / p. 468-473 : ill https://pld.ttu.ee/dildis/publications/IWK'2004_res_inv.pdf

Research in digital design and test at Tallinn University of Technology

Ubar, Raimund-Johannes; Jervan, Gert; Jutman, Artur; Raik, Jaan; Ellervee, Peeter; Kruus, Margus Radioelectronics & informatics 2008 / p. 4-12 : ill <http://www.ewdtest.com/ri/%E2%84%96-1-40-january-march-2008/>

Research on digital system design and test at Tallinn University of Technology

Ubar, Raimund-Johannes; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert; Jutman, Artur; Kruus, Margus; Raik, Jaan Research in Estonia : present and future 2011 / p. 184-205 : ill

Ringhääling '99 : VI Rahvusvahelise Telekommunikatsioonipäeva konverentsi ettekannete materjalid

1999 https://www.ester.ee/record=b1260725*est

Ringhääling 2003 : X rahvusvahelise telekommunikatsioonipäeva materjalid : [16. mai 2003, Tallinn]

2003 http://www.ester.ee/record=b1782571*est

RT-level test point insertion for sequential circuits

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes IWoTA 2004 : IEEE 1st International Workshop on Testability Assessment : November 2, 2004, Rennes, France : proceedings 2004 / p. 34-40 : ill <https://ieeexplore.ieee.org/document/1428412>

Scalable algorithm for structural fault collapsing in digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Orasson, Elmet; Raik, Jaan 2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 5-7, 2015, Daejeon, Korea 2015 / p. 171-176 : ill

Second IEEE East-West Design and Test Workshop

Hahanov, Vladimir; **Ubar, Raimund-Johannes** IEEE journal of design & test of computers 2004 / p. 594

Selected issues of modeling, verification and testing of digital systems

Jutman, Artur 2004 https://www.ester.ee/record=b1989760*est

Self-diagnosis in digital systems = Isediagnoosivad digitaalsüsteemid

Kostin, Sergei 2012 https://www.ester.ee/record=b2757857*est

Self-testing of pipe-lined signal processing architectures at-speed

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 25-28 : ill

Sequential circuits BIST with status bit control

Raik, Jaan; Orasson, Elmet; Ubar, Raimund-Johannes Proceedings of the 11th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2004 : Szczecin, Poland, 24-26 June 2004 2004 / p. 507-510 : ill
https://pld.ttu.ee/~raiub/files/aaaaa_pulk/MIXDES/jaan.pdf

Simulation and automated test development system for digital devices

Birger, Alexander BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 293-295

Sissejuhatus digitaaltehnikasse

Lehtla, Madis 2016 http://www.ester.ee/record=b4618200*est

Small and medium-sized seaports on the digital track : tracing digitalisation across the South Baltic region by innovative auditing procedures

Philipp, Robert; Gerlitz, Laima; Moldabekova, Aisulu Reliability and statistics in transportation and communication : Selected Papers from the 19th International Conference on Reliability and Statistics in Transportation and Communication, RelStat'19, 16-19 October 2019, Riga, Latvia 2020 / p. 351-362 https://doi.org/10.1007/978-3-030-44610-9_35 [Article collection metrics at Scopus](#) [Article at Scopus](#)

Some new aspects of digital filtering

Trump, Tõnu 1993 http://www.ester.ee/record=b1065194*est

Some new aspects of digital filtering : a thesis ... for the degree of doctor of engineering

Trump, Tõnu 1993 http://www.ester.ee/record=b2677070*est

Specification model and language HSL for digital systems

Frištacky, Norbert; Kacerik, Jozef BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 133-136

Structural decision diagrams in digital test : theory and applications

Ubar, Raimund-Johannes; Raik, Jaan; Jenihhin, Maksim; Jutman, Artur 2024 <https://doi.org/10.1007/978-3-031-44734-1>
https://www.ester.ee/record=b5734441*est

Structural test generation with employment of multiple observation time strategy

Skobtsov, Vadim BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 299-302: ill

Structurally synthesized multiple input BDDs for simulation of digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunisia, 13-19 December, 2009 2009 / p. 451-454 : ill
<http://dx.doi.org/10.1109/ICECS.2009.5410895>

Symbolic test generation for hierarchically modeled digital systems

Zaugarov, Viktor 1993 https://www.ester.ee/record=b2090336*est

Synthesis of high-level decision diagrams for functional test pattern generation

Ubar, Raimund-Johannes; Raik, Jaan; Karputkin, Anton; Tombak, Mati Proceedings of the 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009 : Lodz, Poland, 25-27 June, 2009 2009 / p. 519-524 : ill

Synthesis of testable FSM through decomposition

Devadze, Sergei; Sudnitsõn, Aleksander Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 101-104 : ill

Teaching advanced test issues in digital electronics

Ubar, Raimund-Johannes; Orasson, Elmet; Raik, Jaan; Wuttke, Heinz-Dietrich Proceedings of the 6th IEEE International Conference on Information Technology Based Higher Education and Training : ITHET : July 7-9, 2005, Juan Dolio, Dominican Republic 2005 / p. S2B-1 - S2B-6 : ill <http://dx.doi.org/10.1109/ITHET.2005.1560318>

Teaching diagnostic modeling of digital systems with decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Raik, Jaan; Mironov, Dmitri; Evartson, Teet; Orasson, Elmet; Aarna, Margit; Wuttke, Heinz-Dietrich
Proceedings of 12th IASTED International Conference on Computers and Advanced Technology in Education - CATE 2009 :
St.Thomas, US, November 22-24, 2009 2009 / p. 1-6. [CD-ROM]

Teaching research in the laboratory using diagnosis environment for digital systems

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan; Aarna, Margit; Brik, Marina; Wuttke, Heinz-Dietrich 2009 EAAEIE annual
conference : 20th Annual Conference of the European Association for Education in Electrical and Information Engineering : Valencia,
Spain, June 22-24, 2009 2009 / p. 280-283 <https://ieeexplore.ieee.org/document/5335462>

Tehissüsteemide veakindlusest : [TTÜ arvutitehnika instituudi teadustöödest]

Ubar, Raimund-Johannes Horisont 2006 / 2, lk. 64-69 : ill https://artiklid.elnet.ee/record=b2039558*est

Tehted digitaalseadmeis : õppeabimaterjal

Ariste, Andri 1976 https://www.ester.ee/record=b1292367*est

Test cover calculation in digital systems with word-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina Вестник Томского государственного университета 2002 / с.
315-319 : ил

Test generation for control faults in digital systems

Dušina, Julia; Brik, Marina BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994,
Tallinn (Estonia). 1 1994 / p. 325-330: ill

Test generation for digital systems

Ubar, Raimund-Johannes Digest of papers - FTCS 13th Annual International Symposium on Fault-Tolerant Computing, June 28 -
30, 1983, Milano, Italy 1983 / p. 374-377

Test generation for digital systems at functional level

Ubar, Raimund-Johannes; Kuchcinski, Ktysztof; Peng, Z. Research report LiTH-IDA-R-90-06, Linköping University, Sweden 1990
/ p. 1-21

Test generation for digital systems based on alternative graphs

Ubar, Raimund-Johannes Dependable Computing - EDCC-1 : First European Dependable Computing Conference, Berlin,
Germany, October 1994 : proceedings 1994 / p. 151-164: ill

Test generation for sequential digital systems based on symbolic simulation

Skobtsov, Vadim; Skobtsov, Yu. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9,
1998, Tallinn, Estonia : proceedings 1998 / p. 341-344: ill

Testability analysis of digital design verification

Hahanov, V.; Kaminska, M.; **Fomina, Jelena** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of
Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 171-174 :
ill

The current state of voice over Internet protocol in wireless mesh networks

Meeran, Mohammad Tariq; **Annus, Paul; Le Moullec, Yannick** 2016 International Conference on Advances in Computing,
Communications and Informatics (ICACCI) : September 21-24, 2016, The LNM Institute of Information Technology (LNMIT), Jaipur,
India 2016 / p. 2567-2575 : ill <https://doi.org/10.1109/ICACCI.2016.7732444>

The dildis-project-using applets for more demonstrative lectures in digital systems design and test

Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of the 31st ASEE/IEEE Frontiers in Educations Conference :
FIE'2001 : Reno, Nevada 2001 / p. SIE-2-7 <https://ieeexplore.ieee.org/document/963996>

The dildis-project-using applets for more demonstrative lectures in digital systems design and test

Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich FIE 2001 : 31st Annual Frontiers in Educations Conference : Impact on
Engineering and Science Education : Reno, Nevada, October 10-13, 2001 : conference program 2001 / p. 83
<https://ieeexplore.ieee.org/document/963996>

The increasing role of digital technologies in co-production [Online resource]

Lember, Veiko 2017 <http://technologygovernance.eu/files/main/2017090403424444.pdf>

A tool for random test generation targeting high diagnostic resolution

Osimiry, Emmanuel Ovie; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes BEC 2016 : 2016 15th Biennial Baltic
Electronics Conference : proceedings of the 15th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 3-

5, 2016, Tallinn, Estonia 2016 / p. 79-82 : ill http://www.ester.ee/record=b2150914*est

True path tracing in structurally synthesized BDDs for testability analysis of digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Oyeniran, Adeboye Stephen; Jenihhin, Maksim Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 492-499 : ill <https://doi.org/10.1109/DSD.2019.00077>

TTBist: a DFT tool for enhancing functional test for SoC

Hermann, K.; **Raik, Jaan; Jenihhin, Maksim** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 191-194 : ill

Using simulation statistics for bug localization in RTL designs

Tihhomirov, Valentin; Jenihhin, Maksim; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 107-110 : ill

Using test pattern generation tool decider in hardware verification

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 166-169 : ill

Uued meetodid digitaalsüsteemide disaini ja diagnostika valdkonnas : kommentaar Eesti Vabariigi teaduse aastapreemia pälvinud tööle

Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 1998 1999 / lk. 142-145

Web-based software implementation of finite state machine decomposition for design and education

Devadze, Sergei; Kruus, Margus; Sudnitsõn, Aleksander CompSysTech' 2001 : proceedings of the International Conference on Computer Systems and Technologies, Sofia, 21-22 June 2001 2001 / [6] p. : ill https://pld.ttu.ee/decomposition/publications/Sudnitson_CST_Estonia.pdf

Web-based tool for FSM encoding targeting low-power FPGA implementation

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Tarletski, Konstantin 2010 27th International Conference on Microelectronics : MIEL 2010 : Niš, Serbia, 16-19 May 2010 : proceedings 2010 / p. 349-352 <https://ieeexplore.ieee.org/document/5490468>

Web-based training system for teaching digital design and test

Devadze, Sergei 7th International Student Conference on Electrical Engineering : POSTER2003 : May 22, 2003, Prague, Czech Republic 2003 / p. IC6

WebTT - digitaalskeemide testimine ja diagnostikaalaste õppelaborite e-keskkond : [TTÜ arvutitehnika instituut esitles e-Ülikooli konverentsil kolme õppetöös kasutatavat süsteemi]

Robal, Tarmo; Orasson, Elmet Mente et Manu 2005 / 5. mai, lk. 5 : fot https://www.ester.ee/record=b1242496*est

Vector decision diagrams for simulation of digital systems

Ubar, Raimund-Johannes; Morawiec, Adam; Raik, Jaan DDECS'2000 2000 / p. 44-51

Vektorielle alternative graphen und Fehlerdiagnose für digitale Systeme

Ubar, Raimund-Johannes Nachrichtentechnik, Elektronik : technisch-wissenschaftliche Zeitschrift für die gesamte elektronische Nachrichtentechnik 1981 / p. 25-28 : ill https://www.ester.ee/record=b1550811*est

Verification and error correction on High-Level Decision Diagrams

Karputkin, Anton 2013

Verification formelle des resultats de la synthese de Haut Niveau : [doktoriväitekirj]

Dušina, Julia 1999

VHDL based test generation system

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 5th Electronic Devices and Systems Conference, Brno, June 11-12, 1998 1998 / p. 145-148

Über einige Probleme der Testsatzanalyse für digitale Systeme

Ubar, Raimund-Johannes Nachrichtentechnik, Elektronik : technisch-wissenschaftliche Zeitschrift für die gesamte elektronische Nachrichtentechnik 1977 / p. 149-150 https://www.ester.ee/record=b1550811*est

Über einige Probleme der Testsatzanalyse für digitale Systeme

Ubar, Raimund-Johannes Wissenschaftliche Zeitschrift 1976 / p. 447-449 https://www.ester.ee/record=b1516616*est

Автоматизация поверки цифровых вольтметров

Mägi, Harri; Rüstern, Ennu Труды по электротехнике и автоматике : сборник статей. 12 1974 / с. 95-102 : илл
https://www.ester.ee/record=b2190668*est <https://digikogu.taltech.ee/et/Item/57b94a1f-6879-4443-b6f2-322fd7e53d89>

Автоматический синтез тестов для диагностики цифровых устройств

Lohuaru, Tõnu; Pall, Martin; Ubar, Raimund-Johannes Eesti NSV Teaduste Akadeemia toimetised. Füüsika. Matemaatika = Известия Академии наук Эстонской ССР. Физика. Математика = Proceedings of Academy of Sciences of the Estonian SSR. Physics. Mathematics 1983 / lk. 84-94 https://www.ester.ee/record=b1264310*est

Анализ диагностических тестов для комбинационных цифровых схем методом обратного прослеживания неисправностей

Ubar, Raimund-Johannes Автоматика и телемеханика 1977 / с. 168-176 https://www.ester.ee/record=b1515055*est

Быстродействующее устройство выборки и хранения

Gurjanov, Boris; Lavrov, Mihhail; Tamm, Uljas Всесоюзный симпозиум «Проблемы цифрового кодирования и преобразования изображений», г. Тбилиси, 1980 г. : тезисы докладов и программа 1980 / [с. ?]

Генерирование групповых тестов для цифровых схем на модели альтернативных графов

Kivi, E.; Ubar, Raimund-Johannes Тезисы докладов XXXI студенческой научно-технической конференции 1980 / с. 52-55
https://www.ester.ee/record=b1319482*est

Генерирование тестов для комбинационных схем с кратными неисправностями

Ubar, Raimund-Johannes Вопросы проектирования и расчета автоматических информационных систем : [Сборник статей] 1978 / с. 6-10

Дедуктивный анализ тестов в синхронных цифровых схемах без обратных связей

Viilup, Agu; Kitsnik, Peeter; Ubar, Raimund-Johannes Материалы конференции "Автоматизация технического проектирования ЦВМ" (май-июнь 1977 г.) 1977 / с. 178-181

Декомпозиционный метод синтеза контролепригодных цифровых автоматов

Kruus, Margus Машинное проектирование электронных устройств и систем 1986 / с. 52-56

Единый подход к синтезу тестов цифровых схем и систем

Ubar, Raimund-Johannes Межреспубликанская школа-семинар по технической диагностике, 8-12 октября 1984 года : тезисы докладов 1984 / с. 75-81 : илл https://www.ester.ee/record=b1237891*est

Интегрирующие цифровые электромагнитные расходомеры

Gerasimtšuk, Valeri; Meister, Ants 4 Symposium Maritime Elektronik, Messelektronik, 20-22. Apr. 1983, Rostok 1983 / S. 36-44

Интегрирующие цифровые электромагнитные расходомеры

Gerasimtšuk, Valeri; Meister, Ants IX Таллинское совещание по электромагнитным расходомерам : тезисы докладов 1982 / с.34 https://www.ester.ee/record=b1309155*est

Исследование и разработка методов анализа диагностических тестов для цифровых схем : автореферат ... кандидата технических наук (05.13.01)

Kitsnik, Peeter 1981 https://www.ester.ee/record=b1337813*est

Исследование и разработка методов анализа диагностических тестов для цифровых схем : диссертация на соискание ученой степени кандидата технических наук (05.13.01)

Kitsnik, Peeter 1980 https://www.ester.ee/record=b4632972*est

Исследование и разработка методов управления поиском дефектов в цифровых схемах : автореферат кандидата технических наук (05.13.01)

Evartson, Teet 1986 https://www.ester.ee/record=b1301665*est

Метод алгоритмического генерирования тестов при контроле цифровых схем

Grigorjeva, Ksenja; Lohuaru, Tõnu; Evartson, Teet Синтез и диагностика цифровых устройств и систем 1982 / с. 75-83 : илл
https://www.ester.ee/record=b1328194*est <https://digikogu.taltech.ee/et/Item/febd586e-d7fa-4fbd-bf41-40576a75f94b>

Метод локализации неисправностей при проверке цифровых схем автоматическими тестерами

Viilup, Agu; Lohuaru, Tõnu; Ubar, Raimund-Johannes Анализ и моделирование технических устройств и систем АСУТП 1977 / с. 37-45 : илл https://www.ester.ee/record=b2190987*est <https://digikogu.taltech.ee/et/Item/b7c66054-0b4f-4684-9453-442bc7e6e200>

О генерировании тестов цифровых схем в реальном времени

Grigorjeva, Ksenja; Ubar, Raimund-Johannes XVII областная научно-техническая конференция по вопросам повышения

эффективности и качества систем и средств управления (май 1981 года) : тезисы докладов 1981 / с. 112

О системе алгоритмов цифровых устройств

Jänes, Mart Методы машинного проектирования цифровых устройств и систем : материалы краткосрочного семинара, 14-15 июня 1977 / с. 5-8

Об автоматическом синтезе тестов для цифровых объектов систем управления

Plakk, Mari; Ubar, Raimund-Johannes VII Всесоюзное совещание по проблемам управления, Минск, 21-25 ноября 1977. Кн. 3 1977 / с. 97-98

Об одном подходе к моделированию цифровых схем, содержащих счетные структуры

Evertson, Teet; Mištšenko, Andrei Проектирование и диагностика вычислительных средств 1987 / с. 53-63 : илл
https://www.ester.ee/record=b1273275*est

Обобщенная модель альтернативных графов для синтеза тестов цифровых систем

Ubar, Raimund-Johannes Расчет и проектирование систем технической кибернетики 1983 / с. 97-109 : ил
https://www.ester.ee/record=b1288991*est <https://digikogu.taltech.ee/et/Item/7d7515af-76b7-4d35-89a7-e80367d5b635>

Обобщенный подход к многозначному моделированию цифровых схем на модели альтернативных графов

Voolaine, Andrus; Pall, Martin; Ubar, Raimund-Johannes Синтез и диагностика цифровых устройств и систем 1982 / с. 23-37 : илл
https://www.ester.ee/record=b1328194*est <https://digikogu.taltech.ee/et/Item/febd586e-d7fa-4fbd-bf41-40576a75f94b>

Описание неисправностей цифровых устройств

Ubar, Raimund-Johannes Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 3-9 : илл
https://www.ester.ee/record=b1264145*est <https://digikogu.taltech.ee/et/Item/81bf2178-a9f8-417d-86c7-2000cca6a01e>

Описание цифровых устройств моделью альтернативных графов

Ubar, Raimund-Johannes Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 11-33 : илл
https://www.ester.ee/record=b1281890*est <https://digikogu.taltech.ee/et/Item/8e0abfe2-9020-4ebd-85d1-fd67de0d1b30>

Оптимизация процессов диагностирования цифровых устройств в реальном времени

Grigorjeva, Ksenja; Lohuaru, Tõnu; Evertson, Teet; Ubar, Raimund-Johannes Вычислительная техника : тезисы докладов республиканской конференции "Автоматизированное техническое проектирование электронной аппаратуры" (1-2 июня 1982 г.) 1982 / с. 144

Организация процесса анализа тестов цифровых схем на модели альтернативных графов

Voolaine, Andrus; Kitsnik, Peeter; Pall, Martin Вычислительная техника : тезисы докладов республиканской конференции "Автоматизированное техническое проектирование электронной аппаратуры" (1-2 июня 1982 г.) 1982 / с. 34-35

Организация тестовых экспериментов цифровых систем на основе модели альтернативных графов

Lohuaru, Tõnu Межреспубликанская школа-семинар по технической диагностике, 8-12 октября 1984 года : тезисы докладов 1984 / с. 47-52 https://www.ester.ee/record=b1237891*est

Персональная среда проектирование цифровых систем

Raud, Rein; Lohuaru, Tõnu; Ubar, Raimund-Johannes Автоматизация проектирования электронной аппаратуры : Межвузовский тематический научный сборник 1989 / с. 39-43

Проектирование контролепригодных дискретных систем : учебное пособие

Ubar, Raimund-Johannes 1988 https://www.ester.ee/record=b1225400*est

Проектирование контрольных экспериментов в автоматизированной системе контроля цифровых автоматов "НАКС"

Voolaine, Andrus; Jõgi, Aksel; Pall, Martin Синтез и диагностика цифровых устройств и систем 1982 / с. 3-21 : илл
https://www.ester.ee/record=b1328194*est <https://digikogu.taltech.ee/et/Item/febd586e-d7fa-4fbd-bf41-40576a75f94b>

Профессиональная среда проектирования цифровых систем

Raud, R.; Lohuaru, Tõnu; Ubar, Raimund-Johannes Автоматизация проектирования электронной аппаратуры : межвузовский тематический научный сборник 1989 / с. 39-43

Решение задач диагностики цифровых устройств модели альтернативных графов

Kurilova, L.; Popova, S.; Tulina, M.; Ubar, Raimund-Johannes; Jakubovič, M. XXV студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР, 21-23 апреля 1981 года : тезисы докладов. Том 2, Автоматика. Энергетика. Механика. Химия 1981 / с. 39 https://www.ester.ee/record=b1322629*est

Синтез и диагностика цифровых устройств и систем

1982 https://www.ester.ee/record=b1328194*est <https://digikogu.taltech.ee/et/Item/febd586e-d7fa-4fbd-bf41-40576a75f94b>

Синтез тестов для цифровых схем

Plakk, Mari; Ubar, Raimund-Johannes XIV областная научно-техническая конференция по системам и средствам управления (май 1978 г.) : тезисы докладов 1978 / с. 78-79

Система автоматизированной поверки АЦП и ЦВ Е 101

Rüstern, Ennu; Takis, N. Аналого-цифровые и цифро-аналоговые преобразователи : тезисы докладов Республиканской научно-технической конференции, посвященной дню радио, в октябре 1983 года : секция: прецизионные аналого-цифровые и цифро-аналоговые преобразователи 1983 / с. 67-69 : ил https://www.ester.ee/record=b1373964*est

Структурные схемы и алгоритмы работы цифровых систем регулирования

Kracht, Wilhelm XX научная конференция, посвященная 25-летию Эстонской ССР 18-22 мая 1965 г. : тезисы и резюме 1965 / с. 65 https://www.ester.ee/record=b1359832*est

Тестовая диагностика цифровых устройств : учебное пособие. II, Синтез и анализ тестов. Дешифрация диагностических экспериментов

Ubar, Raimund-Johannes 1981 https://www.ester.ee/record=b1326795*est

Управление процессом поиска дефектов в цифровых схемах содержащих счётные структуры

Viilup, Agu; Ubar, Raimund-Johannes; Evertson, Teet Межреспубликанская школа-семинар по технической диагностике, 8-12 октября 1984 года : тезисы докладов 1984 / с. 28-32 https://www.ester.ee/record=b1237891*est