

A new testability calculation method to guide RTL test generation

Raik, Jaan; Nõmmeots, Tanel; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2005 / p. 71-82 : ill <https://doi.org/10.1007/s10836-005-5288-5>

An improved test generation approach for sequential circuits using decision diagrams

Brik, Marina; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 155-158: ill

Application of high-level decision diagrams for simulation-based verification tasks

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Estonian journal of engineering 2010 / 1, p. 56-77 : ill

Application of structurally synthesized binary decision diagrams for timing simulation of digital circuits

Jutman, Artur; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 2001 / 4, p. 269-288 : ill

Assertion checking with PSL and high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Digest of papers IEEE 8th Workshop on RTL and High Level Testing : WRTL'07 : October 12-13, 2007, Beijing, China 2007 / p. 105-110 : ill
https://pld.ttu.ee/~maksim/phd_papers/%5B12%5D%20wrtl%2707.pdf

Automated correction of design errors by edge redirection on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan 13th International Symposium on Quality Electronic Design (ISQED), 2012 2012 / p. 686-693 : ill <https://ieeexplore.ieee.org/document/6113980>

Automated design error debug using high-level decision diagrams and mutation operators

Raik, Jaan; Repinski, Urmas; Tšepurov, Anton; Hantson, Hanno; Ubar, Raimund-Johannes; Jenihhin, Maksim Microprocessors and microsystems 2013 / p. 505-513 : ill <https://doi.org/10.1016/j.micpro.2012.11.004> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Automated software-based self-test generation for microprocessors

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton Proceedings of the 24st International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2017 : Bydgoszcz, Poland, June 19-21, 2014 2017 / p. 453-458 : ill
<https://doi.org/10.23919/MIXDES.2017.8005252>

Automated test program synthesis for digital systems with high-level decision diagrams

Ubar, Raimund-Johannes Proc. of 7th International Conference 2005 / p. 171-180

Automatic generation of EFSMs and HLDDs for functional ATPG

Tšepurov, Anton; Guglielmo, Giuseppe di; Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 143-146 : ill

Boolean derivatives and multi-valued simulation on binary decision diagrams

Ubar, Raimund-Johannes Proceedings of the 4th International Workshop Mixed Design of Integrated Circuits and Systems : MIXDES'97 : Poznan, Poland, 12-14 June 1997 1997 / p. 115-120

Calculation of testability measures on structurally synthesized binary decision diagrams

Ubar, Raimund-Johannes; Heinlaid, J.; Raik, Jaan; Raun, L. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 179-182: ill

Canonical representations of high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Raik, Jaan; Tombak, Mati Estonian journal of engineering 2010 / 1, p. 39-55 : ill

Code coverage analysis on high level decision diagrams

Reinsalu, Uljana Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 56-59 : ill

Code coverage analysis using high-level decision diagrams [Electronic resource]

Raik, Jaan; Reinsalu, Uljana; Ubar, Raimund-Johannes; Jenihhin, Maksim; Ellervee, Peeter 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 201-207 : ill. [CD-ROM]
<https://ieeexplore.ieee.org/document/4538786>

Compaction of decision diagrams for describing multi-process VHDL descriptions

Leveugle, R.; Saucier, Gabriele; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 195-198: ill

Cycle-based simulation with decision diagrams

Ubar, Raimund-Johannes; Morawiec, Adam; **Raik, Jaan** Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 454-458: ill <https://ieeexplore.ieee.org/document/761165>

DECIDER : a decision diagram based hierarchical test generation system

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 2nd International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Szczyrk, Poland, September 2-4, 1998 1998 / p. 269-273
<https://www.ida.liu.se/labs/eslab/publications/pap/db/DDECS98.pdf>

DECIDER : a system for hierarchical test pattern generation

Raik, Jaan; Ubar, Raimund-Johannes Radioelectronics and informatics 2003 / p. 40-45 : ill
https://www.researchgate.net/publication/250395975_DECIDER_A_System_for_Hierarchical_Test_Pattern_Generation

A decision diagram based hierarchical test pattern generator

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 159-162: ill

Decision diagrams - from a mathematical notion to engineering applications

Stankovic, Radomir S.; **Ubar, Raimund-Johannes**; Astola, Jaakko Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 281-301 : ill <http://dx.doi.org/10.2298/FUEE1103281S>

Decision diagrams and digital test

Ubar, Raimund-Johannes ECMS 2003 : 6th International Workshop on Electronics, Control, Measurement and Signals : Liberec, Czechia, June 2-4, 2003 2003 / p. 266-273 : ill [http://www.midem-drustvo.si/Journal%20papers/MIDEM_35\(2005\)4p187.pdf](http://www.midem-drustvo.si/Journal%20papers/MIDEM_35(2005)4p187.pdf)

Decision diagrams and digital test

Ubar, Raimund-Johannes 41th International Conference on Microelectronics, Devices and Materials : MIDEM 2005 : Ribno at Bled, Slovenia : invited plenary paper 2005 / p. 15-26

Decision diagrams for diagnostic modeling

Ubar, Raimund-Johannes MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 43

Dependability evaluation in fault-tolerant systems with high-level decision diagrams

Ubar, Raimund-Johannes; Jervan, Gert; Raik, Jaan; Jenihhin, Maksim; Ellervee, Peeter Computer Science Meets Automation : 10-13 September 2007 : proceedings. Volume II 2007 / p. 147-152 : ill https://www.db-thueringen.de/receive/dbt_mods_00008864

Design error diagnosis using backtrace algorithm on decision diagrams

Repinski, Urmas; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

Diagnostic modeling of digital systems with low- and high-level decision diagrams

Ubar, Raimund-Johannes LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [1] p

Diagnostic modeling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill https://www.researchgate.net/publication/344994231_Diagnostic_Modeling_of_Digital_Systems_with_Multi-Level_Decision_Diagrams

Diagnostic modeling of microprocessors with high-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Brik, Marina; Istenberg, Martin; Wuttke, Heinz-Dietrich BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 147-150 : ill

Diagnostic modelling of digital systems with binary and high-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Kruus, Helena; Lensen, Harri; Evertson, Teet Progress in industrial mathematics at ECMI 2006 2008 / p. 902-907 : ill https://link.springer.com/chapter/10.1007/978-3-540-71992-2_158

Diagnostic modelling of digital systems with decision diagrams

Ubar, Raimund-Johannes Вестник Томского государственного университета : приложение 2004 / август, материалы международных, всесоюзных и региональных научных конференций, симпозиумов, школ, проводимых в ТГУ, с. 174-179 : ил

Diagnostic modelling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Evertson, Teet; Kruus, Margus; Lensen, Harri Proceedings of the 17th IASTED International Conference on Modelling and Simulation : May 24-26, 2006, Montreal, Quebec, Canada 2006 / p. 207-212 : ill

Digitaalsüsteemide diagnostika Tallinna Tehnikaülikoolis

Ubar, Raimund-Johannes Teadusmõtte Eestis : tehnikateadused 2002 / lk. 107-113 : ill

Dynamic analysis of digital circuits with 5-valued simulation

Ubar, Raimund-Johannes Mixed design of integrated circuits and systems 1998 / p. 187-192: ill

https://link.springer.com/chapter/10.1007/978-1-4615-5651-0_29

Equivalent transformations of structurally synthesized BDDs and applications

Jürimägi, Lembit; Ubar, Raimund-Johannes; Viies, Vladimir 2019 8th Mediterranean Conference on Embedded Computing (MECO) 2019 / 6 p. : ill <https://doi.org/10.1109/MECO.2019.8760283>

Fast RTL fault simulation using decision diagrams and bitwise set operations

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes; Ellervee, Peeter 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 3-5 October 2011, Vancouver, Canada 2011 / p. 164-170

<https://ieeexplore.ieee.org/document/6104440>

Fault effect reasoning in digital systems by topological view on low- and high-level decision diagrams

Ubar, Raimund-Johannes Вестник Томского государственного университета. Управление, вычислительная техника и информатика 2014 / p. 99-113 : ill http://journals.tsu.ru/informatics/&journal_page=archive&id=923&article_id=12107

Fault modeling and test generation with low- and high-level decision diagrams

Ubar, Raimund-Johannes 24. GI/GMM/ITG-Workshop : Testmethoden und Zuverlässigkeit von Schaltungen und Systemen 2012 / p. 1-12

Fault simulation and code coverage analysis of RTL designs using high-level decision diagrams = Rikete simuleerimine ja koodikatte analüüs register-siirde tasemel kasutades kõrgtaseme otsustusdiagramme

Reinsalu, Uljana 2013 https://www.ester.ee/record=b2963595*est

Fault simulation with parallel critical path tracing for combinational circuits using structurally synthesized BDDs

Devadze, Sergei; Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 97-102 : ill

Formal verification and error correction on high-level decision diagrams = Formaalne verifitseerimine ja vigade parandamine kõrgtasemelistel otsustusdiagrammidel

Karputkin, Anton 2012

FPGA design flow with automated test generation

Elst, G.; Diener, Karl-Heinz; Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes Proc. of German 11th Workshop on Test Technology and Reliability of Circuits and Systems : Potsdam, 1999 1999 / p. 120-123

<https://masters.donntu.ru/2010/fknt/masyakin/library/article7.pdf>

Generation of tests for the localization of single gate design errors in combinational circuits using the stuck-at fault model

Ubar, Raimund-Johannes; Borriane, Dominique XI Brazilian Symposium on Integrated Circuit Design, September 30 - October 3, 1998, Rio de Janeiro, Brazil : proceedings 1998 / p. 51-54 <https://ieeexplore.ieee.org/document/715409>

Hierarchical calculation of malicious faults for evaluating the fault-tolerance

Ubar, Raimund-Johannes; Devadze, Sergei; Jenihhin, Maksim; Raik, Jaan; Jervan, Gert; Ellervee, Peeter Proceedings : Fourth IEEE International Symposium on Electronic Design, Test and Applications : [DELTA 2008] : 23-25 January 2008, Hong Kong, SAR, China 2008 / p. 222-227 : ill <https://ieeexplore.ieee.org/document/4459544>

Hierarchical fault diagnosis in embedded digital systems with multi-level decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Evertson, Teet; Lensen, Harri; Aarna, Margit 5th International Conference on Industrial Automation = Cinquieme Conference Internationale sur l'Automatisation Industrielle : June 11-13, 2007, Montreal, Canada 2007 / [6] p. [CD-ROM]

Hierarchical test generation with multi-level decision diagram models

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 7th IEEE North Atlantic Test Workshop, West Greenwich RI, USA, May 28-29, 1998 1998 / p. 26-33

https://www.academia.edu/67811738/Hierarchical_Test_Generation_with_Multi_Level_Decision_Diagram_Models?hb-g-sw=7883185

High level decision diagrams and characteristic polynomials

Karputkin, Anton Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 143-146 : ill

High-level decision diagram based fault models for targeting FSMs

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 353-358 : ill <http://dx.doi.org/10.1109/DSD.2006.60>

High-Level Decision Diagram manipulations for code coverage analysis

Minakova, Karina; Reinsalu, Uljana; Tšepurov, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level decision diagram simulation for diagnosis and soft-error analysis

Raik, Jaan; Repinski, Urmass; Jenihhin, Maksim; Tšepurov, Anton Design and test technology for dependable systems-on-chip 2011 / p. 294-309 : ill <https://www.igi-global.com/chapter/high-level-decision-diagram-simulation/51406>

High-level decision diagrams based coverage metrics for verification and test

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes LATW 2009 : 10th IEEE Latin American Test Workshop : Buzios, Rio de Janeiro, Brazil, March 2-5, 2009 2009 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2009.4813792>

High-level decision diagrams for improving simulation performance of digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Morawiec, Adam SCI 2000 : World Multiconference on Systemics, Cybernetics and Informatics : July 23-26, 2000, Orlando, Florida, USA : proceedings. Volume IX, Industrial Systems 2000 / p. 62-67 : ill <https://hal.science/hal-01396447v1>

High-level design error diagnosis using backtrace on decision diagrams

Raik, Jaan; Repinski, Urmass; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton 28th Norchip Conference : Tampere, Finland, 15-16 November 2010 : conference program and papers 2010 / [4] p. : ill <http://dx.doi.org/10.1109/NORCHIP.2010.5669486>

How to generate high quality tests for digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Kruus, Helena; Raik, Jaan 2004 International Semiconductor Conference : 27th edition, October 4-6, 2004, Sinaia, Romania : CAS 2004 proceedings. Volume 2 2004 / p. 459-462 : ill <http://dx.doi.org/10.1109/SMICND.2004.1403048>

Intelligent decision making approach for performance evaluation of a robot-based manufacturing cell

Kangru, Tavo; Riives, Jüri; Otto, Tauno; Pohlak, Meelis; Mahmood, Kashif ASME 2018 International Mechanical Engineering Congress and Exposition : Pittsburgh, Pennsylvania, USA, November 9–15, 2018 2018 / Paper No. IMECE2018-86666, pp. V002T02A092; 10 p. : ill <http://doi.org/10.1115/IMECE2018-86666>

Mixed hierarchical-functional fault models for targeting sequential cores

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Jenihhin, Maksim Journal of systems architecture 2008 / 3/4, p. 465-477 : ill <https://www.sciencedirect.com/science/article/abs/pii/S1383762107001166>

Modeling microprocessor faults on high-level decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Istenberg, Martin; Wuttke, Heinz-Dietrich DSN 2008 : supplemental : 2008 IEEE International Conference on Dependable Systems & Networks With FTCS & DCC (DSN) : June 24-27, 2008, Anchorage, Alaska 2008 / p. C17-C22 : ill. [CD-ROM] [https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08\(LAAS\)_files/Slides/WDSN08S-04-Ubar.pdf](https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08(LAAS)_files/Slides/WDSN08S-04-Ubar.pdf)

Multi-level fault simulation of digital systems on decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina The First IEEE International Workshop on Electronic Design, Test and Applications : DELTA 2002, 29-31 January 2002, Christchurch, New Zealand : proceedings 2002 / p. 86-91 : ill

Multiple fault testing in systems-on-chip with high-level decision diagrams

Ubar, Raimund-Johannes; Oyeniran, Adeboye Stephen; Schölzel, Mario; Vierhaus, Heinrich Theodor Proceedings of 2015 10th International Design & Test Symposium (IDT) : Dead Sea, Jordan, 14-16 December 2015 2015 / p. 66-71 : ill <http://dx.doi.org/10.1109/IDT.2015.7396738>

Multi-valued simulation of digital circuits with structurally synthesized binary decision diagrams

Ubar, Raimund-Johannes Multiple valued logic. Vol. 4 1998 / p. 141-157

Multi-valued simulation with binary decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan Proceedings IEEE European Test Workshop, Cagliari, Italy, May 28-30, 1997 1997 / p. 28-29

Mutation analysis with high-level decision diagrams

Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Tšepurov, Anton; Ubar, Raimund-Johannes; Guglielmo, Giuseppe di; Fummi, Franco LATW2010 : 11th Latin-American TestWorkshop, March 28-31, 2010, Punta del Este, Uruguay 2010 / [6] p. [CD-

ROM] <https://ieeexplore.ieee.org/document/5550336>

New fault models and self-test generation for microprocessors using High-Level Decision Diagrams

Jasnetski, Artjom; **Raik, Jaan; Tšertov, Anton; Ubar, Raimund-Johannes** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 251-254 : ill

New method of testability calculation to guide RT-level test generation

Raik, Jaan; Nõmmeots, Tanel; Ubar, Raimund-Johannes 4th IEEE Latin-American Test Workshop : LATW2003 : Natal, Brazil, February 16-19, 2003 2003 / p. 46-51 : ill <https://link.springer.com/article/10.1007/s10836-005-5288-5>

On automatic software-based self-test program generation based on high-Level decision diagrams

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 177 <http://dx.doi.org/10.1109/LATW.2016.7483357>

On SSBDD model size & complexity

Jutman, Artur ECS'03 : proceedings of the 4th Electronic Circuits and Systems Conference : September 11-12, 2003, Bratislava, Slovakia 2003 / p. 17-22 https://pld.ttu.ee/~artur/papers/SSBDD_Model_Size-ECS03.pdf

Optimization of structurally synthesized BDDs

Ubar, Raimund-Johannes; Vassiljeva, T.; Raik, Jaan; Jutman, Artur; Tombak, Mati; Peder, Ahti Proceedings of the Fourth IASTED International Conference on Modelling, Simulation, and Optimization : August 17-19, 2004, Kawai, Hawaii, USA 2004 / p. 234-240 : ill https://www.academia.edu/22101496/Optimization_of_structurally_synthesized_BDDs

Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems

Ubar, Raimund-Johannes Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 303-324 : ill <http://dx.doi.org/10.2298/FUEE1103303U>

Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems

Ubar, Raimund-Johannes Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 1-10 : ill <https://scindeks-clanci.ceon.rs/data/pdf/0353-3670/2011/0353-36701103303U.pdf>

Parallel fault analysis on structurally synthesized BDDs

Devadze, Sergei; Ubar, Raimund-Johannes Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 47-50 : ill

Probabilistic equivalence checking based on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 423-428 : ill <https://ieeexplore.ieee.org/document/5783130>

PSL assertion checking using temporally extended high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2009 / 6, p. 289-300 : ill https://pld.ttu.ee/home/maksim/phd_papers/%5B11%5D%20latw%2708.pdf

PSL assertion checking with temporally extended high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 49-54 : ill https://pld.ttu.ee/~maksim/phd_papers/%5B11%5D%20latw%2708.pdf

PSL assertions based verification with HLDD tools

Jenihhin, Maksim Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 17-20 : ill

Ranking strategic objectives in a strategy map based on logarithmic fuzzy preference programming and similarity method

Safari, Hossein; Khanmohammadi, Ehsan; Maleki, Meysam; Cruz-Machado, Virgilio; **Ševtšenko, Eduard** Management Systems in Production Engineering 2019 / p. 153-161 : ill <https://doi.org/10.1515/mspe-2019-0025> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Register-transfer level deductive fault simulation using decision diagrams

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 193-196 : ill

Remarks on different decision diagrams

Stankovic, Radomir S.; **Ubar, Raimund-Johannes**; Astola, Jaakko Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 99-110 : ill

Sequential circuit test generation using decision diagram models

Raik, Jaan; Ubar, Raimund-Johannes Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 736-740: ill https://www.cs.york.ac.uk/rts/docs/SIGDA-Compendium-1994-2004/papers/1999/date99/pdf/files/11e_1.pdf

Simulation-based verification with APRICOT framework using high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 13-16 : ill

SoC and board modeling for processor-centric board testing

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 14th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2011 : 31 August - 2 September 2011, Oulu, Finland : proceedings 2011 / p. 575-582 : ill <https://ieeexplore.ieee.org/document/6037463>

Software-based self-test generation for microprocessors with high-level decision diagrams

Ubar, Raimund-Johannes; Tšertov, Anton; Jasnetski, Artjom; Brik, Marina LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Software-based self-test generation for microprocessors with high-level decision diagrams

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton; Brik, Marina Proceedings of the Estonian Academy of Sciences 2014 / p. 48-61 : ill https://artiklid.elnet.ee/record=b2665215*est <https://doi.org/10.3176/proc.2014.1.08> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Software-based self-test with decision diagrams for microprocessors

Ubar, Raimund-Johannes; Jasnetski, Artjom; Tšertov, Anton; Oyeniran, Adeboye Stephen 2018

Structural decision diagrams in digital test : theory and applications

Ubar, Raimund-Johannes; Raik, Jaan; Jenihhin, Maksim; Jutman, Artur 2024 <https://doi.org/10.1007/978-3-031-44734-1> https://www.ester.ee/record=b5734441*est

Structural fault collapsing by superposition of BDDs for test generation in digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur Proceedings of the Eleventh International Symposium on Quality Electronic Design ISQED 2010 : March 22-24, 2010 San Jose, California USA 2010 / p. 250-257 : ill <https://ieeexplore.ieee.org/document/5450451>

Structurally synthesized binary decision diagrams

Jutman, Artur; Peder, Ahti; Raik, Jaan; Tombak, Mati; Ubar, Raimund-Johannes Boolean Problems : 6th International Workshop : September 23-24, 2004, Freiberg 2004 / p. 271-278 : ill

Structurally synthesized multiple input BDDs for simulation of digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunisia, 13-19 December, 2009 2009 / p. 451-454 : ill <http://dx.doi.org/10.1109/ICECS.2009.5410895>

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation

Leveugle, R.; **Ubar, Raimund-Johannes** Electron technology 1999 / 3, p. 282-287 : ill

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation

Leveugle, R.; **Ubar, Raimund-Johannes** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 353-358 <https://hal.science/ccsd-00015077/>

Synthesis of high-level decision diagrams for functional test pattern generation

Ubar, Raimund-Johannes; Raik, Jaan; Karputkin, Anton; Tombak, Mati Proceedings of the 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009 : Lodz, Poland, 25-27 June, 2009 2009 / p. 519-524 : ill

Teaching diagnostic modeling of digital systems with decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Raik, Jaan; Mironov, Dmitri; Evartson, Teet; Orasson, Elmet; Aarna, Margit; Wuttke, Heinz-Dietrich Proceedings of 12th IASTED International Conference on Computers and Advanced Technology in Education - CATE 2009 : St. Thomas, US, November 22-24, 2009 2009 / p. 1-6. [CD-ROM]

Temporally extended high-level decision diagrams for PSL assertions simulation

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings : Thirteenth IEEE European Test Symposium : ETS 2008 : 25-29 May 2008, Verbania, Italy 2008 / p. 61-68 : ill <https://ieeexplore.ieee.org/document/4556029>

Testability calculation for digital circuits with decision diagrams

Ubar, Raimund-Johannes 3rd IEEE Latin American Test Workshop : LATW'02, Montevideo, Uruguay, February 10-13, 2002 : digest of papers 2002 / p. 137-143 : ill <https://dblp.org/rec/conf/latw/Ubar02.html>

Testability guided hierarchical test generation with decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Nõmmeots, Tanel 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 / p. 265-271 <https://www.semanticscholar.org/paper/Testability-Guided-Hierarchical-Test-Generation-Ubar-Raik/c6301ac35d003c92f3867f26e2e75b87e1ad9b47>

Timing simulation of digital circuits with binary decision diagrams

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. Design, Automation and Test in Europe : Conference and Exhibition 2001 : Munich, Germany, March 13-16, 2001 : proceedings 2001 / p. 460-466 : ill <https://ieeexplore.ieee.org/document/915063>

True path tracing in structurally synthesized BDDs for testability analysis of digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Oyeniran, Adeboye Stephen; Jenihhin, Maksim Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 492-499 : ill <https://doi.org/10.1109/DSD.2019.00077>

Using test pattern generation tool decider in hardware verification

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 166-169 : ill

Vector decision diagrams for simulation of digital systems

Ubar, Raimund-Johannes; Morawiec, Adam; Raik, Jaan DDECS'2000 2000 / p. 44-51

Verification and error correction on High-Level Decision Diagrams

Karputkin, Anton 2013