

Composing graph theory and deep neural networks to evaluate SEU type soft error effects

Balakrishnan, Aneesh; Lange, Thomas; Glorieux, Maximilien; Alexandrescu, Dan; **Jenihhin, Maksim** 9th Mediterranean Conference on Embedded Computing (MECO'2020), Budva, Montenegro, 8-11 June 2020 2020
<https://doi.org/10.1109/MECO49872.2020.9134279>

Enabling cross-layer reliability and functional safety assessment through ML-based compact models

Alexandrescu, Dan; **Balakrishnan, Aneesh**; Lange, Thomas; Glorieux, Maximilien Proceedings : 2020 26th IEEE International Symposium on On-Line Testing and Robust System Design : IOLTS 2020, Napoli, Italy, July 13-16, 2020 : virtual edition 2020 / 6 p. : ill <https://doi.org/10.1109/IOLTS50870.2020.9159750>

Gate-level graph representation learning : a step towards the improved stuck-at faults analysis

Balakrishnan, Aneesh; **Alexandrescu, Dan**; **Jenihhin, Maksim**; Lange, Thomas; Glorieux, Maximilien Proceedings of the Twenty Second International Symposium on Quality Electronic Design (ISQED) : Santa Clara, USA, 7-9 April 2021 2021 / p. 24-30
<https://doi.org/10.1109/ISQED51717.2021.9424256>

Machine learning clustering techniques for selective mitigation of critical design features

Lange, Thomas; **Balakrishnan, Aneesh**; Glorieux, Maximilien; Alexandrescu, Dan; Sterpone, Luca Proceedings : 2020 26th IEEE International Symposium on On-Line Testing and Robust System Design : IOLTS 2020, Napoli, Italy, July 13-16, 2020 : virtual edition 2020 / 7 p. : ill <https://doi.org/10.1109/IOLTS50870.2020.9159751>

Machine learning to tackle the challenges of transient and soft errors in complex circuits

Lange, Thomas; **Balakrishnan, Aneesh**; Glorieux, Maximilien; Alexandrescu, Dan; Sterpone, Luca 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS), 1-3 July 2019, Greece 2019 / p. 7-14 : ill
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Modeling gate-level abstraction hierarchy using graph convolutional neural networks to predict functional de-rating factors

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On the estimation of complex circuits functional failure rate by machine learning techniques

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The validation of graph model-based, gate level low-dimensional feature data for machine learning applications

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