

A DFT scheme to improve coverage of hard-to-detect faults in FinFET SRAMs

Cardoso Medeiros, Guilherme; **Gürsoy, Cemil Cem**; Fieback, Moritz; Wu, Lizhou; **Jenihhin, Maksim**; Taouil, Mottaqiallah; Hamdioui, Said 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE), 9-13 March 2020, Grenoble, France : proceedings 2020 / p. 792-797 <https://doi.org/10.23919/DATE48585.2020.9116278>

High-level combined deterministic and pseudo-exhaustive test generation for RISC processors

Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Gürsoy, Cemil Cem**; **Raik, Jaan** 2019 IEEE European Test Symposium (ETS) : proceedings 2019 / 6 p. : ill <https://doi.org/10.1109/ETS.2019.8791526>

Mixed-level identification of fault redundancy in microprocessors

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New categories of Safe Faults in a processor-based Embedded System

Gürsoy, Cemil Cem; **Jenihhin, Maksim**; **Oyeniran, Adeboye Stephen**; Piumatti, Davide; **Raik, Jaan**; Sonza Reorda, Matteo; **Ubar, Raimund-Johannes** 2019 22nd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Cluj-Napoca, Romania : proceedings 2019 / 4 p. : ill <https://doi.org/10.1109/DDECS.2019.8724642>

On BTI aging rejuvenation in memory address decoders

Gürsoy, Cemil Cem; Kraak, Daniel; **Ahmed, Foisal**; Taouil, Mottaqiallah; **Jenihhin, Maksim**; Hamdioui, Said 2022 IEEE 23rd Latin American Test Symposium, LATS 2022 2022 / Code 184360 <https://doi.org/10.1109/LATS57337.2022.9936940>

On NBTI-induced aging analysis in IEEE 1687 reconfigurable scan networks

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RESCUE EDA Toolset for interdependent aspects of reliability, security and quality in nanoelectronic systems design

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Software-based mitigation for memory address decoder aging

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