Analysis of defect tolerant crossbar network implementations
Leveugle, R.; Brahic, P. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 37-40: ill

Behavior modeling of faulty complex VLSIs : why and how?
Leveugle, R. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 191-194: ill

Compaction of decision diagrams for describing multi-process VHDL descriptions
Leveugle, R.; Saucier, Gabriele; **Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 195-198: ill

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation
Leveugle, R.; **Ubar, Raimund-Johannes** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 353-358

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation
Leveugle, R.; **Ubar, Raimund-Johannes** Electron technology 1999 / 3, p. 282-287 : ill