

Fast test pattern generation for sequential circuits using decision diagram representations

Raik, Jaan; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications (JETTA) 2000 / 3, p. 213-226 : ill
<https://link.springer.com/article/10.1023/A:1008335130158>

Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits

Jenihhin, Maksim; Squillero, Giovanni; Tihomirov, Valentin; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill <https://doi.org/10.1007/s10836-016-5589-x> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Identifying untestable faults in sequential circuits using test path constraints

Viilukas, Taavi; Karputkin, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill <https://link.springer.com/article/10.1007/s10836-012-5312-5>

Optimization of boundary scan tests using FPGA-based efficient scan architectures

Aleksejev, Igor; Devadze, Sergei; Jutman, Artur; Shibin, Konstantin Journal of electronic testing : theory and applications (JETTA) 2016 / p. 245-255 : ill <https://doi.org/10.1007/s10836-016-5588-y> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)