

### **A new approach to build a low-level malicious fault list starting from high-level description and alternative graphs**

Benso, A.; Prinetto, Paolo; Rebaudengo, M.; Sonza, M.; **Ubar, Raimund-Johannes** Proceedings IEEE European Design & Test Conference, Paris, March 17-20, 1997 1997 / p. 560-565 <https://ieeexplore.ieee.org/document/582417>

### **Exploiting high-level descriptions for circuits fault tolerance assessments**

Benso, A.; Prinetto, Paolo; Rebaudengo, M.; Sonza Reorda, Matteo; **Raik, Jaan; Ubar, Raimund-Johannes** 1997 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Paris, October 20-22, 1997 1997 / p. 212-216 <https://ieeexplore.ieee.org/document/628327>

### **Foreword**

**Ubar, Raimund-Johannes**; Prinetto, Paolo; Al-Hashimi, Bashir Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005 2005 / p. III

### **10th IEEE European Test Symposium**

**Ubar, Raimund-Johannes**; Prinetto, Paolo; **Raik, Jaan** IEEE journal of design & test of computers 2005 / p. 480-481 : phot <http://dx.doi.org/10.1109/MDT.2005.106>