

From FPGAs to obfuscated eASICs : design and security trade-offs

Abideen, Zain Ul; Perez, Tiago Diadami; Pagliarini, Samuel Nascimento IEEE Asian Hardware-Oriented Security and Trust (AsianHOST) 2021 / p. 1-4 <https://doi.org/10.1109/AsianHOST53231.2021.9699758>

A security-aware and LUT-based CAD flow for the physical synthesis of hASICs

Abideen, Zain Ul; Perez, Tiago Diadami; Martins, Mayler; Pagliarini, Samuel Nascimento IEEE transactions on computer-aided design of integrated circuits and systems 2023 / p. 3157-3170 : ill <https://doi.org/10.1109/TCAD.2023.3244879> [Journal metrics at Scopus](#)
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