CMOS defects analysis using DefSim measurement environment
Pleskacz, Witold A.; Borejko, Tomasz; Walkanis, A.; Stopjakova, Viera; **Jutman, Artur**; **Ubar, Raimund-Johannes** Informal Digest of Papers : Eleventh IEEE European Test Symposium : ETS 2006 : 21-24 May 2006, Southampton, United Kingdom 2006 / p. 241-246 : ill

DefSim: a remote laboratory for studying physical defects in CMOS digital circuits
Pleskacz, Witold A.; Stopjakova, Viera; Borejko, Tomasz; **Jutman, Artur**; Walkanis, Andrzej IEEE transactions on industrial electronics 2008 / 6, p. 2405-2415 : ill
https://www.researchgate.net/publication/3219964_DefSim_A_Remote_Laboratory_for_Studying_Physical_Defects_in_CMOS_Digital_Circuits

DefSim: CMOS defects on chip for research and education
Pleskacz, Witold A.; Borejko, Tomasz; Walkanis, A.; Stopjakova, Viera; **Jutman, Artur**; **Ubar, Raimund-Johannes** 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 74-79 : ill

DefSim: measurement environment for CMOS defects
Borejko, Tomasz; **Jutman, Artur**; Pleskacz, Witold A.; **Ubar, Raimund-Johannes** 2006 25th International Conference on Microelectronics : Belgrade, Serbia and Montenegro, 14-17 May 2006 : proceedings. Volume 2 2006 / p. 679-682
https://ieeexplore.ieee.org/document/1651048