

A VLSI implementation of RSA and IDEA encryption engine

Buldas, Ahto; Pöldre, Jüri Proceedings [of the] 15th NORCHIP Conference, Tallinn, 10-11 November 1997 1997 / p. 281-288: ill

At-speed testing and test quality evaluation for high-performance pipelined systems Töökiirusel testimine ja testi kvaliteedi hindamine kõrgjõudlus-konveierarhitektuuriga süsteemidele

Gorev, Maksim 2015 <https://digi.lib.ttu.ee/1/23953>

Automatic test generation system for VLSI

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the First Electronic Circuits and Systems Conference : Bratislava, Slovakia, September 4-5, 1997 1997 / p. 255-258

Behavior modeling of faulty complex VLSIs : why and how?

Leveugle, R. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 191-194: ill

CAD of CCD VLSI

Zaycev, S.N.; Kanunnikov, A.I.; Pugachev, A.A.; Shilin, V.A. Automation, simulation & measurement : 3rd biennial conference : Tallinn, Estonia, October 7-11, 1991. Section S, Simulation = Automatiseerimine, modelleerimine ja mõõtmine : 3. rahvusvaheline konverents / Tallinna Tehnikaülikool 1992 / p. 120-122: ill https://www.ester.ee/record=b1064031*est

Compaction of decision diagrams for describing multi-process VHDL descriptions

Leveugle, R.; Saucier, Gabriele; **Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 195-198: ill

Control intensive digital system synthesis

Tammemäe, Kalle 1997 http://www.ester.ee/record=b1060033*est

Current conveyor based structures for continuous-time MOS filters

Piccirilli, Maria Cristina BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 359-362: ill

DeepHLS: A complete toolchain for automatic synthesis of deep neural networks to FPGA

Riazati, Mohammad; Daneshtalab, Masoud; Sjodin, Mikael; Lisper, Bjorn ICECS 2020 - 27th IEEE International Conference on Electronics, Circuits and Systems, November 23-25, 2020, Virtual Conference : Proceedings 2020 / 4 p <https://doi.org/10.1109/ICECS49266.2020.9294881>

Defect-oriented BIST quality analysis

Kruus, Helena; Ubar, Raimund-Johannes; Raik, Jaan BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 153-156 : ill

Dependability improvements of NoC-based systems = Töökindluse parandamine kiipvõrkudel põhinevates süsteemides

Niazmand, Behrad 2018 <https://digi.lib.ttu.ee/1/29879> https://www.ester.ee/record=b4907650*est

Design error diagnosis with re-synthesis in combinational circuits

Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2003 / 1, p. 73-82 : ill <https://link.springer.com/article/10.1023/A:1021948013402>

Design obfuscation versus test

Farahmandi, Farimah; Sinanoglu, Ozgur; Blanton, Ronald; **Pagliarini, Samuel Nascimento** 2020 IEEE European Test Symposium (ETS) : ETS 2020, May 25 - 29, 2020, Tallinn, Estonia 2020 / 10 p <https://doi.org/10.1109/ETS48528.2020.9131590>

Design of a configurable order statistic filter in CMOS VLSI

Hu, M.; Vainio, Olli BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 305-308: ill

Design space exploration and optimisation for NoC-based timing sensitive systems

Tagel, Mihkel; **Ellervee, Peeter; Jervan, Gert** BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 177-180 : ill

Design-aid programs for LSI integrated circuits

Tarnay, K.; Szekely, V.; Baji, P.; Farkas, G.; Masszi, F.; Kerecsen-Rencz, M. Проблемы моделирования и измерения в электронике 1986 / p. 3-11

Digital logic simulation with compressed BDDs

Ubar, Raimund-Johannes; Mironov, Dmitri; Devadze, Sergei; Raik, Jaan Proceedings : 2011 IEEE International Conference on Computer Science and Automation Engineering : June 10-12, 2011, Shanghai, China 2011 / p. 105-109 : ill
<https://ieeexplore.ieee.org/document/5952643>

Digital test in WEB-based environment

Ivask, Eero 2006 https://www.ester.ee/record=b2158119*est

An efficient systolic array algorithm for memory-based VLSI array implementation of DST

Chiper, Doru-Florin BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 265-268: ill

Fault diagnosis of VLSI devices using alternative graph representation

Ubar, Raimund-Johannes Proceedings of the 8th Symposium on Microcomputer and Microprocessor Applications, Budapest, October 12-14, 1994. Vol. 1 1994 / p. 34-44

FPGA design flow with automated test generation

Elst, G.; Diener, Karl-Heinz; **Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes** Proc. of German 11th Workshop on Test Technology and Reliability of Circuits and Systems : Potsdam, 1999 1999 / p. 120-123
<https://masters.donntu.ru/2010/fknt/masyakin/library/article7.pdf>

Functional test generation for finite state machines

Ubar, Raimund-Johannes; Brik, Marina; Jutman, Artur; Raik, Jaan; Bengtsson, Tomas; Kumar, Shashi BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 205-208 : ill

A general approach to synthesis of the finite-state machine logical structure in the sum-of-products form

Chapenko, V.; Fritsnovich, G.; Kalnberzin, A.; Lange, E. BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 2 1994 / p. 385-390 https://www.ester.ee/record=b2150914*est

Generic interconnect BIST for Network-on-Chip

Jutman, Artur; Ubar, Raimund-Johannes; Raik, Jaan DDECS : 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 13-16, 2005, Sopron, Hungary : proceedings 2005 / p. 224-227 : ill

Graph embedding in boolean hypercube

Fomina, Jelena; Zakrevskij, Arkadij BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 131-134 : ill

Hierarchical test generation for finite state machines

Brik, Marina; Ubar, Raimund-Johannes BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 319-324: ill

High-level synthesis of control and memory intensive applications : thesis submitted to the Royal Institute of Technology in partial fulfillment of the requirements for the degree of Doctor of Technology

Ellervee, Peeter 2000

Hybrid built-in self-test : methods and tools for analysis and optimization of BIST = Sisseehitatud hübriidne isetestimine : meetodid ja vahendid analüüsiks ning optimeerimiseks

Orasson, Elmet 2007 https://www.ester.ee/record=b2305436*est

Multi-level test generation and fault diagnosis for finite state machines

Ubar, Raimund-Johannes; Brik, Marina Dependable computing : proceedings / EDCC-2, Second European Dependable Computing Conference, Taormina, Italy, October 2-4, 1996 1996 / p. 264-281: ill

A new modified berger code for concurrent error detection

Maamar, Ali H.; Russel, Gordon BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 187-190: ill

On SSBDD model size & complexity

Jutman, Artur ECS'03 : proceedings of the 4th Electronic Circuits and Systems Conference : September 11-12, 2003, Bratislava, Slovakia 2003 / p. 17-22 https://pld.ttu.ee/~artur/papers/SSBDD_Model_Size-ECS03.pdf

Optimization of built-in self-test in digital systems = Sisseehitatud enesetestimise optimeerimine digitaalsüsteemides

Kruus, Helena 2011

Probabilistic analysis of CMOS physical defects in VLSI circuits for test coverage improvement

Blyzniuk, M.; Kazymyra, I.; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Microelectronics reliability 2001 / p. 2023-2040 : ill <https://www.sciencedirect.com/science/article/pii/S0026271401000920>

Representing transparency conditions in test generation for VLSI by decision diagrams

Ubar, Raimund-Johannes Proceedings of the First Electronic Circuits and Systems Conference : Bratislava, Slovakia, September 4-5, 1997 1997 / p. 213-216

Riistvara kirjeldamiskeel - VHDL : metoodiline materjal

Tammemäe, Kalle 2003 http://www.ester.ee/record=b1605950*est

Riistvara kirjeldamiskeel VHDL : metoodiline materjal

Tammemäe, Kalle 2002 http://www.ester.ee/record=b1605950*est

Runtime contention and bandwidth-aware adaptive routing selection strategies for networks-on-chip

Samman, Faizal; **Hollstein, Thomas**; Glesner, Manfred IEEE transactions on parallel and distributed systems 2013 / p. 1411-1421 : ill <https://doi.org/10.1109/TPDS.2012.200> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

System-level design of timing-sensitive network-on-chip based dependable systems = Kiipvõrkudel põhinevate ajakriitiliste ja töökindlate süsteemide kõrgtaseme disain

Tagel, Mihkel 2012 https://www.ester.ee/record=b2778263*est

Test synthesis from register-transfer level descriptions

Raik, Jaan; Paomets, Priidu BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 311-314: ill

The optimization, design and performance of the FBCM23 ASIC for the upgraded CMS beam monitoring system

Kaplon, Jan; Wegrzyn, Grzegorz; **Shibin, Konstantin**; Barendregt, Marnix Journal of instrumentation 2024 / art. C02026, 6 p. : ill <https://doi.org/10.1088/1748-0221/19/02/C02026> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Conference proceedings at WOS](#) [Article at WOS](#)

Turbo tester : a CAD system for teaching digital test

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Microelectronics education : proceedings of the 2nd European Workshop held in Noordwijkerhout, The Netherlands, 14-15 May 1998 1998 / p. 287-290: ill https://link.springer.com/chapter/10.1007/978-94-011-5110-8_66

VLSI kõrgtaseme süntees

Tammemäe, Kalle Arvutustehnika ja Andmetöötlus 1993 / 1, lk. 25-31

VLSI system level codesign toolkit AKKA

Tammemäe, Kalle; O'Nils, Mattias; Tornemo, Anders; Tenhunen, Hannu NORCHIP Conference '96 : 14th conference, Helsinki, 4-5 November 1996 1996 / p. 1-7: ill https://www.researchgate.net/publication/2407722_VLSI_system_level_codesign_toolkit_AKKA

xTractor : an academic high-level synthesis tool for control and memory intensive applications

Ellervee, Peeter University Booth at Design and Test in Europe : DATE'05 : Munich, Germany, 2005 2005 / ? p <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=6db1d71884b75b47fb27ae86b91b61894e57fd18>

Проектирование контролепригодных дискретных систем : учебное пособие

Ubar, Raimund-Johannes 1988 https://www.ester.ee/record=b1225400*est