Formalization of finite state machines with data path for the verification of high-level synthesis

Borrione, Dominique; **Dušina, Julia**; Pierre, Laurence XI Brasilian Symposium on Integrated Circuit Design, September 30 - October 3, 1998, Rio de Janeiro, Brazil : proceedings 1998 / p. 99-102: ill https://ieeexplore.ieee.org/document/715419

Generation of tests for the localization of single gate design errors in combinational circuits using the stuck-at fault model **Ubar, Raimund-Johannes**; Borrione, Dominique XI Brasilian Symposium on Integrated Circuit Design, September 30 - October 3, 1998, Rio de Janeiro, Brazil: proceedings 1998 / p. 51-54 https://ieeexplore.ieee.org/document/715409