

Automatic synthesis of asynchronous circuits from synchronous RTL descriptions

Öberg, Johnny; Plosila, Juha; **Ellervee, Peeter** Proceedings 23rd NORCHIP Conference : Oulu, Finland, 21-22 November 2005 2005 / p. 200-205 : ill <https://ieeexplore.ieee.org/document/1597024/keywords#keywords>

DyMeP : an infrastructure to support dynamic memory binding for runtime mapping in CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter**; Hemani, Ahmed; Tenhunen, Hannu; Plosila, Juha Doctoral School in Information and Communication Technology : proceedings of doctoral session of BEC 2014 : October 6-8 2014, Laulasmaa 2014 / Ik. 19-22 : ill

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Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter**; Hemani, Ahmed; Tenhunen, Hannu; Plosila, Juha 28th International Conference on VLSI Design : held concurrently with 14th International Conference on Embedded Systems : 3-7 January 2015, Bangalore, India : proceedings 2015 / p. 547-552 : ill <https://doi.org/10.1109/VLSID.2015.98> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Polymorphic configuration architecture for CGRAs

Jafri, Syed Mohammad Asad Hassan; **Tajammul, Muhammad Adeel**; Hermani, Ahmed; Paul, Kolin; Plosila, Juha; **Ellervee, Peeter**; Tenhunen, Hannu IEEE transactions on Very Large Scale Integration (VLSI) Systems 2016 / p. 403-407 : ill <http://dx.doi.org/10.1109/TVLSI.2015.2402392>