A scalable model based RTL framework zamiaCAD for static analysis
Tšepurov, Anton; **Jenihhin, Maksim**; **Raik, Jaan**; **Tihhomirov, Valentin** 2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC) : October 7-10, 2012 Santa Cruz, USA Dream Inn, Santa Cruz, USA : [proceedings] 2012 / p. 171-176 : ill https://www.semanticscholar.org/paper/A-scalable-model-based-RTL-framework-zamiaCAD-for-Tsepurov-Bartsch/d19eefa44f793621d537c06498784e06e0332fd2

Abstraction of clock interface for conversion of RTL VHDL to SystemC
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** 2014 IEEE International Advance Computing Conference (IACC) : February 21-22, 2014, Gurgaon, India 2014 / p. 50-55 : ill

Extensible open-source framework for translating RTL VHDL IP cores to SystemC
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

Performance analysis of cosimulating processor core in VHDL and SystemC
Saif Abrar, Syed; Shyam Kiran A.; **Jenihhin, Maksim**; **Raik, Jaan**; Babu, C. Proceedings of the 2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 22–25 August 2013, Mysore, India 2013 / p. 563-568 : ill