

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]

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Combinational fault simulation in sequential circuits

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Comparison of two approaches to improve functional BIST fault coverage

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Environment for the analysis of functional self-test quality in digital systems

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Functional self-test of high-performance pipe-lined signal processing architectures

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Parallel critical path tracing fault simulation in sequential circuits

Kõusaar, Jaak; Ubar, Raimund-Johannes; Kostin, Sergei; Devadze, Sergei; Raik, Jaan Proceedings of 25th International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS : MIXDES 2018 : Gdynia, Poland, June 21-23, 2018 2018 / p. 305-310 : ill <https://doi.org/10.23919/MIXDES.2018.8436880>

Self-testing of pipe-lined signal processing architectures at-speed

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