An automatic approach to evaluate assertions' quality based on data-mining metrics
Ghasempouri, Tara; **Niazmand, Behrad**; **Raik, Jaan** Proceedings 2nd IEEE International Test Conference in Asia : ITC-Asia 2018, 15-17 August 2018, Harbin, China 2018 / p. 61-66 : ill https://doi.org/10.1109/ITC-Asia.2018.00021

Automated area and coverage optimization of minimal latency checkers
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Apneet Kaur**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 2017 22nd IEEE European Test Symposium (ETS 2017), Limassol, Cyprus, 22 – 26 May 2017 : proceedings 2017 / p. 7-8 : ill https://doi.org/10.1109/ETS.2017.7968211

Automated minimization of concurrent online checkers for network-on-chips
Saltarelli, Pietro; **Niazmand, Behrad**; **Hariharan, Ranganathan**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 10th International Symposium on Reconfigurable and Communication-centric Systems-on-Chip (ReCoSoC 2015) : Bremen, 29 June - 1 July 2015 2015 / [8] p. : ill http://dx.doi.org/10.1109/ReCoSoC.2015.7238079

AWAIT : an ultra-lightweight soft-error mitigation mechanism for network-on-chip links
Janson, Karl; **Pihlak, Rene**; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Jervan, Gert**; **Raik, Jaan** 2018 13th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), Lille, France, July 9th-11th, 2018 2018 / p. 1-6 : ill https://doi.org/10.1109/ReCoSoC.2018.8449374

Comprehensive performance and robustness analysis of 2D turn models for network-on-chips
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Janson, Karl**; Kogge, Thilo; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 2017 IEEE International Symposium on Circuits and Systems (ISCAS) 2017 / p. 1476-1479 : ill https://doi.org/10.1109/ISCAS.2017.8050634

Dependability improvements of NoC-based systems = Töökindluse parandamine kiipvõrkudel põhinevates süsteemides
Niazmand, Behrad 2018 https://digi.lib.ttu.ee/i/?9879

Design and verification of secure cache wrapper against access-driven side-channel attacks
Niazmand, Behrad; **Azad, Siavoosh Payandeh**; **Jervan, Gert**; Sepulveda, Johanna Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 672-676 : ill https://doi.org/10.1109/DSD.2019.00108

Enabling secure MPSoC dynamic operation through protected communication
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Jervan, Gert**; Sepulveda, Johanna 2018 25th IEEE International Conference on Electronics Circuits and Systems (ICECS), Bordeaux, France, December 9–12, 2018 2018 / p. 481-484 : ill https://doi.org/10.1109/ICECS.2018.8617940

Extended checkers for control part of routers in network-on-chips
Hariharan, Ranganathan; **Niazmand, Behrad**; **Hollstein, Thomas**; **Raik, Jaan**; **Jervan, Gert** MEDIAN 2015 : the 4th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : March 13, 2015, Grenoble, France 2015 / p. 36-39 : ill

Extended checkers for logic-based distributed routing in network-on-chips
Niazmand, Behrad; **Hariharan, Ranganathan**; **Govind, Vineeth**; **Jervan, Gert**; **Hollstein, Thomas**; **Raik, Jaan** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 83-86 : ill

Extended checkers for logic-based distributed routing in network-on-chips
Niazmand, Behrad; **Hariharan, Ranganathan**; **Govind, Vineeth**; **Jervan, Gert**; **Hollstein, Thomas**; **Raik, Jaan** BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 77-80 : ill

Fault-resilient NoC router with transparent resource allocation
Putkaradze, Tsotne; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Raik, Jaan**; **Jervan, Gert** 12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC2017), July 12-14, 2017, Madrid, Spain : proceedings 2017 / 8 p. : ill https://doi.org/10.1109/ReCoSoC.2017.8016161 https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8016161

A framework for area-efficient concurrent online checkers design
Saltarelli, Pietro; **Niazmand, Behrad**; **Hariharan, Ranganathan**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 64-69 : ill

A framework for combining concurrent checking and online embedded test for low-latency fault detection in NoC routers
Saltarelli, Pietro; **Niazmand, Behrad**; **Raik, Jaan**; **Govind, Vineeth**; **Hollstein, Thomas**; **Jervan, Gert**; **Hariharan, Ranganathan** NOCS '15 : International Symposium on Networks-on-Chip : Vancouver, BC, Canada, September 28-30, 2015 2015 / [8] p. : ill http://dx.doi.org/10.1145/2786572.2788713

A framework for comprehensive automated evaluation of concurrent online checkers
Saltarelli, Pietro; **Niazmand, Behrad**; **Raik, Jaan**; **Hariharan, Ranganathan**; **Jervan, Gert**; **Hollstein, Thomas** Euromicro Conference on Digital System Design : DSD 2015 : 26-28 August 2015, Funchal, Madeira, Portugal : proceedings 2015 / p. 288-292 : ill http://dx.doi.org/10.1109/DSD.2015.15

From online fault detection to fault management in network-on-chips : a ground-up approach
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Janson, Karl**; **Nevin, George**; **Oyeniran, Adeboye Stephen**; **Putkaradze, Tsotne**; **Apneet Kaur**; **Raik, Jaan**; **Jervan, Gert**; **Ubar, Raimund-Johannes**; **Hollstein, Thomas** Proceedings 2017 IEEE 20th International Symposium on Design and Diagnotics of Electronic Circuit & Systems(DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 48-53 : ill https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553

From RTL liveness assertions to cost-effective hardware checkers
Hariharan, Ranganathan; **Ghasempouri, Tara**; **Niazmand, Behrad**; **Raik, Jaan** XXXIII Conference on Design of Circuits and Integrated Systems (DCIS) : proceedings 2018 / 6 p. : ill https://doi.org/10.1109/DCIS.2018.8681487

Handling of SETs on NoC links by exploitation of inherent redundancy in circular input buffers [Online resource]
Janson, Karl; **Pihlak, Rene**; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Jervan, Gert**; **Raik, Jaan** BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p.: ill https://doi.org/10.1109/BEC.2018.8600989

A hierarchical approach for devising area efficient concurrent online checkers
Niazmand, Behrad; **Azad, Siavoosh Payandeh**; **Ghasempouri, Tara**; **Raik, Jaan**; **Jervan, Gert** Proceedings 2nd IEEE International Test Conference in Asia : ITC-Asia 2018, 15-17 August 2018, Harbin, China 2018 / p. 139-144 : ill https://doi.org/10.1109/ITC-Asia.2018.00034

Holistic approach for Fault-Tolerant Network-on-Chip based many-core systems [Online resource]
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** arXiv.org 2016 / [8] p. : ill

LiD-CAT: A lightweight detector for cache ATtacks
Reinbrecht, Cezar; Hamdioui, Said; Taouil, Mottaqiallah; **Niazmand, Behrad**; **Ghasempouri, Tara**; **Raik, Jaan**; Sepulveda, Johanna 2020 IEEE European Test Symposium (ETS) : ETS 2020, May 25-29, 2020 Tallinn, Estonia : proceedings 2020 / 6 p. : ill https://doi.org/10.1109/ETS48528.2020.9131603

Logic-based implementation of fault-tolerant routing in 3D Network-on-Chips
Niazmand, Behrad; **Azad, Siavoosh Payandeh**; Flich, Jose; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 2016 Tenth IEEE/ACM International Symposium on Networks-on-Chip (NOCS) : Nara, Japan, 31 August - 2 September 2016 2016 / [8] p. : ill https://doi.org/10.1109/NOCS.2016.7579317

QoSinNoC: analysis of QoS-aware NoC architectures for mixed-criticality applications
Avramenko, Serhiy; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Raik, Jaan**; **Jenihhin, Maksim** 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 67-72 : ill https://doi.org/10.1109/DDECS.2018.00-10

SoCDep2 : a framework for dependable task deployment on many-core systems under mixed-criticality constraints
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Ellervee, Peeter**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 2016 11th International Symposium on Reconfigurable Communication‐centric Systems‐on‐Chip (ReCoSoC) : June 27‐29, 2016, Tallinn, Estonia 2016 / [6] p. : ill https://doi.org/10.1109/ReCoSoC.2016.7533903

Towards formal verification of cache access-based side-channel attacks
Niazmand, Behrad; Reinbrecht, Cezar; **Raik, Jaan**; **Jervan, Gert**; Sepulveda, Johanna Testmethoden und Zuverlässigkeit von Schaltungen und Systemen, TUZ 2019 2019 / 2 p. : tab http://www.informatik.uni-bremen.de/tuz/2019

Understanding MPSoCs : exploiting memory microarchitectural vulnerabilities of high performance NoC-based MPSoCs
Sepulveda, Johanna; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Jervan, Gert** SAMOS '18 : Proceedings of the 18th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, Pythagorion, Greece, July 15-19, 2018 2018 / p. 162-166 https://doi.org/10.1145/3229631.3239367 Conference proceedings at Scopus Article at Scopus Article at WOS

Upgrading QoSinNoC : efficient routing for mixed-criticality applications and power analysis
Avramenko, Serhiy; **Azad, Siavoosh Payandeh**; Violante, Massimo; Niazmand, Behrad; **Raik, Jaan**; **Jenihhin, Maksim** Proceedings of the 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 8-10, 2018, Verona, Italy 2018 / p. 207-212 : ill https://doi.org/10.1109/VLSI-SoC.2018.8644866