

Logic simulation and fault collapsing with shared structurally synthesized BDDs

Mironov, Dmitri; Ubar, Raimund-Johannes; Raik, Jaan 2014 19th IEEE European Test Symposium (ETS) : May 26th-30th, 2014, Paderborn, Germany : proceedings 2014 / [2] p. : ill

Lower bounds of the size of shared structurally synthesized BDDs

Ubar, Raimund-Johannes; Mironov, Dmitri Proceedings of the 2014 IEEE 17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 23-25, 2014, Warsaw, Poland 2014 / p. 77-82 : ill

A novel fault-tolerant logic style with self-checking capability

Taheri, Mahdi; Sheikhpour, Saeideh; Mahani, Ali; Jenihhin, Maksim Proceedings - 2022 IEEE 28th International Symposium on On-Line Testing and Robust System Design, IOLTS 2022 2022 / art. 183305 : ill <https://doi.org/10.1109/IOLTS56730.2022.9897818>

Structurally synthesized multiple input BDDs for simulation of digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunisia, 13-19 December, 2009 2009 / p. 451-454 : ill <http://dx.doi.org/10.1109/ICECS.2009.5410895>

Timing-critical path analysis with structurally synthesized BDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; Jenihhin, Maksim; Raik, Jaan; Olugbenga, Niyi-Leigh; Viies, Vladimir 2018 7th Mediterranean Conference on Embedded Computing (MECO) 2018 / 6 p. : ill <https://doi.org/10.1109/MECO.2018.8406051>