

Comprehensive abstraction of VHDL RTL cores to ESL SystemC = Register-siirde taseme VHDL kirjelduste kompleksne abstraherimine süsteemitaseme SystemC mudeliteks

Abrar, Syed Saif 2016 http://www.ester.ee/record=b4564850*est

FSMD RTL design manipulation for clock interface abstraction

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 10-13 August 2015, Kerala, India 2015 / p. 463-468 : ill <http://dx.doi.org/10.1109/ICACCI.2015.7275652>

SystemC-based loose models : RTL abstraction for design understanding

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan Workshop on Design Automation for Understanding Hardware Designs DUHDe 2015 : Grenoble, March 13, 2015 2015 / p. 1-6

SystemC-based loose models for simulation speed-up by abstraction of RTL IP cores

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 71-74 : ill <http://dx.doi.org/10.1109/DDECS.2015.39>