

A new evolutionary-technique-based approach to optimize pseudo-random TPG for logic BIST

Jutman, Artur; Aleksejev, Jevgeni; Ubar, Raimund-Johannes MEET/MARIND'2002 : proceedings of First International Congress on Mechanical and Electrical Engineering and Technology and Fourth International Conference on Marine Industry, 07-11 October 2002, Varna Bulgaria. Volume 1 2002 / p. 247-252 : ill

A scalable static test set compaction method for sequential circuits

Aleksejev, Igor; Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 87-92 : ill

A tool for advanced learning of LFSR-based testing principles

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 175-178 : ill

A tool for teaching pseudo-random TPG principles

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes Proceedings of the 17th EAEEIE Annual Conference on Innovation in Education for Electrical and Information Engineering : Craiova, Romania, June 1st-3rd, 2006 2006 / p. 182-187 : ill

An educational environment for digital testing : hardware, tools, and web-based runtime platform

Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes; Vislogubov, Vladislav Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 412-419 : ill https://www.researchgate.net/profile/Artur-Jutman/publication/220880167_An_Educational_Environment_for_Digital_Testing_Hardware_Tools_and_Web-Based_Runtime_Platform/links/02e7e53c3c71b0b2a7000000/An-Educational-Environment-for-Digital-Testing-Hardware-Tools-and-Web-Based-Runtime-Platform.pdf

Analysis of a test method for delay faults in NoC interconnects

Bengtsson, Tomas; Jutman, Artur; Kumar, Shashi; Ubar, Raimund-Johannes; Peng, Zebo Proceedings of the IEEE East-West Design & Test Workshop (EWDWT'06) : Sochi, Russia, September 15-19, 2006 2006 / p. 42-46 : ill

Applets for learning digital design and test [Electronic resource]

Ubar, Raimund-Johannes; Jutman, Artur; Kruus, Margus; Wuttke, Heinz-Dietrich 1st International Conference on Interactive Mobile and Computer Aided Learning (IMCL2006) : Amman, Jordan, April 19-21, 2006 2006 / p. 1-4 : ill. [CD-ROM]

Application of sequential test set compaction to LFSR reseeding

Aleksejev, Igor; Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes 26th Norchip Conference : Tallinn, Estonia, 17-18 November 2008 : formal proceedings 2008 / p. 102-107 : ill <http://dx.doi.org/10.1109/NORCHP.2008.4738292>

Application of structurally synthesized binary decision diagrams for timing simulation of digital circuits

Jutman, Artur; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 2001 / 4, p. 269-288 : ill

Assessment of student's design results in e-learning-scenarios [Electronic resource]

Wuttke, Heinz-Dietrich; Ubar, Raimund-Johannes; Henke, Karsten; Jutman, Artur 8th International Conference on Technology Based Higher Education and Training : 10th to 13th July, 2007, KKR Hotel Kumamoto, Kumamoto, Japan : [proceedings] 2007 / [6] p. [CD-ROM]

Asynchronous e-learning resources for hardware design issues

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of the International Conference on Computer Systems and Technologies (e-learning) : CompSysTech'04 : Rousse, Bulgaria, 17-18 June 2004 / p. IV.11-1 - IV.11-6 : ill https://www.researchgate.net/publication/234797327_Asynchronous_e-learning_resources_for_hardware_design_issues

Asynchronous fault detection in IEEE P1687 instrument network

Shibin, Konstantin; Devadze, Sergei; Jutman, Artur IEEE 23rd North Atlantic Test Workshop : 14-16 May 2014, Binghamton, New York : proceedings 2014 / p. 73-78 : ill

At-speed on-chip diagnosis of board-level interconnect faults

Jutman, Artur Ninth IEEE European Test Symposium : ETS 2004 : 23-26 May 2004, Corsica, France : proceedings 2004 / p. 2-7 : ill https://www.researchgate.net/publication/4098807_At-speed_on-chip_diagnosis_of_board-level_interconnect_faults

Automatic SoC level test path synthesis based on partial functional models

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 2011 Asian Test Symposium (ATS) : New Delhi, India 2011 / p. 532-538 <https://ieeexplore.ieee.org/document/6114730>

Automation of testing beyond the SoCs

Tšertov, Anton; Jutman, Artur; Devadze, Sergei Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda

BASTION : board and SoC test instrumentation for ageing and no failure found

Jutman, Artur; Lotz, Christophe; Larsson, Erik; Sonza Reorda, Matteo; **Jenihhin, Maksim; Raik, Jaan** Proceedings of the 2017 Design, Automation & Test in Europe (DATE) : 27-31 March 2017, Swisstech, Lausanne, Switzerland 2017 / p. 115-120 : ill
<https://doi.org/10.23919/DATE.2017.7926968>

BIST analyzer : a training platform for SoC testing [Electronic resource]

Jutman, Artur; Tšertov, Anton; Tšepurov, Anton; Aleksejev, Igor; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 37th Annual Frontiers in Education Conference : Global Engineering : Knowledge Without Borders, Opportunities Without Passports : Milwaukee, Wisconsin, October 10-13, 2007 2007 / p. S3H-8-S3H-13 : ill. [CD-ROM] <http://dx.doi.org/10.1109/FIE.2007.4418125>

Bringing research issues into lab scenarios on the example of SoC testing [Electronic resource]

Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei; Wuttke, Heinz-Dietrich International Conference on Engineering Education - ICEE 2007 : September 3-7, 2007, Coimbra, Portugal 2007 / [7] p. : ill. [CD-ROM]
<http://icee2007.dei.uc.pt/proceedings/papers/429.pdf>

Calculation of LFSR seed and polynomial pair for BIST applications

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 105-108 : ill

Calculation of LFSR seed and polynomial pair for BIST applications [Electronic resource]

Jutman, Artur; Tšertov, Anton; Ubar, Raimund-Johannes 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 275-279 : ill. [CD-ROM] <https://ieeexplore.ieee.org/abstract/document/4538801>

CMOS defects analysis using DefSim measurement environment

Pleskacz, Witold A.; Borejko, Tomasz; Walkanis, A.; Stopjakova, Viera; **Jutman, Artur; Ubar, Raimund-Johannes** Informal Digest of Papers : Eleventh IEEE European Test Symposium : ETS 2006 : 21-24 May 2006, Southampton, United Kingdom 2006 / p. 241-246 : ill

CMS drift tubes sector collector relocation phase 1 upgrade [Electronic resource]

Bedoya, C. F.; **Jutman, Artur; Shibin, Konstantin; Devadze, Sergei** 2015 http://cms.cern.ch/iCMS/jsp/openfile.jsp?type=DN&year=2015&files=DN2015_011.pdf

DefSim - the defective IC

Pleskacz, Witold A.; **Jutman, Artur; Ubar, Raimund-Johannes; Devadze, Sergei** DATE 2007 : Design Automation and Test in Europe : Nice, France, April 16-20, 2007 2007 / p. s96 (2 p.)

DefSim: a remote laboratory for studying physical defects in CMOS digital circuits

Pleskacz, Witold A.; Stopjakova, Viera; Borejko, Tomasz; **Jutman, Artur;** Walkanis, Andrzej IEEE transactions on industrial electronics 2008 / 6, p. 2405-2415 : ill
https://www.researchgate.net/publication/3219964_DefSim_A_Remote_Laboratory_for_Studying_Physical_Defects_in_CMOS_Digital_Circuits

DefSim: CMOS defects on chip for research and education

Pleskacz, Witold A.; Borejko, Tomasz; Walkanis, A.; Stopjakova, Viera; **Jutman, Artur; Ubar, Raimund-Johannes** 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 74-79 : ill

DefSim: measurement environment for CMOS defects

Borejko, Tomasz; **Jutman, Artur;** Pleskacz, Witold A.; **Ubar, Raimund-Johannes** 2006 25th International Conference on Microelectronics : Belgrade, Serbia and Montenegro, 14-17 May 2006 : proceedings. Volume 2 2006 / p. 679-682
<https://ieeexplore.ieee.org/document/1651048>

DefSim-based exercises for studying defects in CMOS gates

Jutman, Artur; Pleskacz, Witold A.; **Boiko, Nikolai; Ubar, Raimund-Johannes** EWME 2006 proceedings : 6th International Workshop on Microelectronics Education : 8-9 June, 2006, Stockholm, Sweden 2006 / p. 23-26 : ill

Delay testing of asynchronous NoC interconnects

Bengtsson, Tomas; **Jutman, Artur;** Kumar, Shashi; **Ubar, Raimund-Johannes** Proceedings of the 12th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2005 : Krakow, Poland, 22-25 June, 2005. Vol. 1 of 2 2005 / p. 419-424 : ill

Design error diagnosis in digital circuits with stuck-at fault model

Jutman, Artur; Ubar, Raimund-Johannes Microelectronics reliability 2000 / p. 307-320 : ill [https://doi.org/10.1016/S0026-2714\(99\)00203-6](https://doi.org/10.1016/S0026-2714(99)00203-6)

Design error localization in digital circuits by stuck-at fault test patterns

Jutman, Artur; Ubar, Raimund-Johannes [MIEL] 2000 : 22nd International Conference on Microelectronics : Niš, Yugoslavia, 14-

Designing reliable cyber-physical systems

Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; **Devadze, Sergei; Jenihhin, Maksim; Jutman, Artur; Raik, Jaan; Shibin, Konstantin** Languages, design methods, and tools for electronic system design : selected contributions from FDL 2016 2018 / p. 15-38 : ill https://doi.org/10.1007/978-3-319-62920-9_2 [Conference Proceedings at Scopus](#) [Article at Scopus](#)

Designing reliable cyber-physical systems : overview associated to the special session at FDL'16

Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; **Devadze, Sergei; Jenihhin, Maksim; Jutman, Artur; Raik, Jaan; Shibin, Konstantin** The 2016 Forum on Specification & Design Languages : proceedings : Bremen, Germany, September 14-16, 2016 2016 / [8] p. : ill <https://doi.org/10.1109/FDL.2016.7880382>

Diagnostic modeling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill https://www.researchgate.net/publication/344994231_Diagnostic_Modeling_of_Digital_Systems_with_Multi-Level_Decision_Diagrams

Diagnostic modeling of microprocessors with high-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Brik, Marina; Istenberg, Martin; Wuttke, Heinz-Dietrich BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 147-150 : ill

Diagnostic software with WEB interface for teaching purposes

Vislogubov, Vladislav; **Jutman, Artur; Kruus, Helena; Orasson, Elmet; Raik, Jaan; Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 255-258 : ill

DIAGNOZER : a laboratory tool for teaching research in diagnosis of electronic systems [Electronic resource]

Ubar, Raimund-Johannes; Kostin, Sergei; Jutman, Artur; Raik, Jaan; Wuttke, Heinz-Dietrich 2009 IEEE International Conference on Microelectronic Systems Education MSE '09 : 25-27 July 2009, San Francisco, California : [proceedings] 2009 / p. 12-15 : ill. [CD-ROM] <http://dx.doi.org/10.1109/MSE.2009.5270842>

Digital design learning system based on Java applets

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes 4th Annual Conference of the LTSN Centre for Information and Computer Sciences : 26th-28th August 2002, NUI Galway, Ireland 2003 / p. 183-187 : ill <https://pld.ttu.ee/diids/publications/Sudnitson%20LTSN-ICS%202003.pdf>

Digital electronics design and test at Computer Engineering Department of Tallinn University of Technology

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Ellervee, Peeter The house magazine : the parliamentary weekly 2006 / 1198, p. 42 : ill

Distance-learning tools for digital design and test issues

Jutman, Artur; Kruus, Margus; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes IT+SE'2002 : Information Tec[h]nologies in Science, Education, Telecommunication, Business : proceedings = Информационные технологии в науке, образовании, телекоммуникации, бизнесе, Украина, Крым, Ялта-Гурзуф, 20-30 мая 2002 года : труды 2002 / p. 269-272 : ill

Effective scalable IEEE 1687 instrumentation network for fault management

Jutman, Artur; Shibin, Konstantin; Devadze, Sergei IEEE design & test 2013 / p. 26-35 : ill <https://doi.org/10.1109/MDAT.2013.2278535> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Efficient at-speed interconnect BIST and diagnosis framework

Jutman, Artur Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005 2005 / p. 257-258 : ill https://artiklid.elnet.ee/record=b1018804*est

Efficient single-pattern fault simulation on structurally synthesized BDDs

Raik, Jaan; Ubar, Raimund-Johannes; Devadze, Sergei; Jutman, Artur Dependable Computing - EDCC-5 : 5th European Dependable Computing Conference : Budapest, Hungary, April 20-22, 2005 : proceedings 2005 / p. 332-344 : ill

Efficient TPG for a fast at-speed interconnect BIST [Electronic resource]

Jutman, Artur 7th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 18-21, 2004, Stará Lesná, Slovakia : proceedings 2004 / p. 223-226 : ill. [CD-ROM]

E-learning environment for WEB-based study of testing

Ubar, Raimund-Johannes; Jutman, Artur; Raik, Jaan; Devadze, Sergei; Jenihhin, Maksim; Alekseev, Igor; Tšepurov, Anton; Tšertov, Anton; Kostin, Sergei; Orasson, Elmet; Wuttke, Heinz-Dietrich Proceedings of the 8th European Workshop on Microelectronics Education : EWME 2010 : Darmstadt, Germany, 10-12 May 2010 2010 / p. 47-52 : ill

E-learning environment in the area of digital microelectronics

Jutman, Artur; Sudnitsön, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich ITHET 2004 : proceedings of the Fifth International Conference on Information Technology based Higher Education and Training : 31 May - 2 June, 2004, Istanbul, Turkey 2004 / p. 278-283 : ill

E-learning tools for digital test

Devadze, Sergei; Gorjachev, R.; Jutman, Artur; Orasson, Elmet; Rosin, Vjatšeslav; Ubar, Raimund-Johannes Proc. III International Conference "Distance Learning - Educational Sphere of XXI Century" : Minsk, Belorussia, 2003 2003 / p. 336-342

E-learning tools for teaching self-test of digital electronics

Jutman, Artur; Gramatova, Elena; Pikula, T.; Ubar, Raimund-Johannes 15 EAEIE International Conference on Innovation in Education for Electrical and Information Engineering : Sofia, Bulgaria, May 27-29, 2004 2004 / p. 267-272 : ill

Embedded instrumentation toolbox for screening marginal defects and outliers for production

Odintsov, Sergei; Jutman, Artur; Devadze, Sergei; Aleksejev, Igor IEEE AUTOTESTCON 2017 : Schaumburg, USA, Sept 11-14, 2017 : proceedings 2017 / p. 336-334 : ill <https://doi.org/10.1109/AUTEST.2017.8080516>

Embedded synthetic instruments for board-level testing

Jutman, Artur; Devadze, Sergei; Aleksejev, Igor; Wenzel, Thomas Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th-June 1st, 2012, Annecy, France 2012 / 1 p. : ill <https://ieeexplore.ieee.org/document/6233044>

Exact static compaction of independent test sequences

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 315-318 : ill

Exact static compaction of sequential circuit tests using branch-and-bound and search state registration

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes ETW'02 : 7th IEEE European Test Workshop, Gorfu Greece, May 26-29, 2002 : informal digest 2002 / p. 19-20
https://www.researchgate.net/publication/250423148_Exact_Static_Compaction_of_Sequential_Circuit_Tests_Using_Branch-and-Bound_and_Search_State_Registration

Fast and efficient static compaction of test sequences based on greedy algorithms

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Győr, Hungary, April 18-20, 2001 2001 / p. 117-122 https://slideplayer.com/slide/9971880/#google_vignette

Fast extended test access via JTAG and FPGAs

Devadze, Sergei; Jutman, Artur; Aleksejev, Igor; Ubar, Raimund-Johannes International Test Conference 2009 : November 1 - November 6, 2009, Austin Convention Center, Austin, Texas USA : proceedings 2009 / p. 1-7 : ill
<http://dx.doi.org/10.1109/TEST.2009.5355668>

Fast fault simulation for extended class of faults in scan-path circuits

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur Proceedings : Fifth IEEE International Symposium on Electronic Design, Test and Applications : DELTA 2010 : 13-15 January 2010, Ho Chi Minh City, Vietnam 2010 / p. 14-19
<https://ieeexplore.ieee.org/document/5438717>

Fast static compaction of test sequences using implications and greedy search

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes ETW 2001 : IEEE European Test Workshop : Stockholm, May 29 June 1, 2001 : informal digest 2001 / p. 207-209 : ill <https://www.semanticscholar.org/paper/Fast-Static-Compaction-of-Test-Sequences-using-and-Raik-Jutman/3a7a8ddda6e63d3e2fde0c8650d4518851746221>

Fast static compaction of tests composed of independent sequences : basic properties and comparison of methods

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes The 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS 2002 : September 15-18, 2002, Dubrovnik, Croatia. Volume II 2002 / p. 445-448 : ill
<http://dx.doi.org/10.1109/ICECS.2002.1046190> <https://ieeexplore.ieee.org/document/1046190>

Fault collapsing with linear complexity in digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS 2010) : 30 May - 2 June 2010, Paris, France 2010 / p. 653-656 : ill
<https://ieeexplore.ieee.org/document/5537504>

Fault management instrumentation network based on IEEE P1687 JTAG

Shibin, Konstantin; Jutman, Artur; Devadze, Sergei European Test Symposium (ETS), 2013, Avignon, France 2013

Fault simulation with parallel critical path tracing for combinational circuits using structurally synthesized BDDs

Devadze, Sergei; Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 97-102 : ill

FPGA-based embedded virtual instrumentation = FPGA-sisened virtuaalsed test- ja mõõtevahendid

Aleksejev, Igor 2013 http://www.ester.ee/record=b2927687*est

FPGA-based synthetic instrumentation for board test

Aleksejev, Igor; Jutman, Artur; Devadze, Sergei; Odintsov, Sergei; Wenzel, Thomas Proceedings : International Test Conference 2012 2012 / p. 1-10 : ill <https://ieeexplore.ieee.org/document/6401571>

Functional test generation for finite state machines

Ubar, Raimund-Johannes; Brik, Marina; Jutman, Artur; Raik, Jaan; Bengtsson, Tomas; Kumar, Shashi BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 205-208 : ill

Generic interconnect BIST for Network-on-Chip

Jutman, Artur; Ubar, Raimund-Johannes; Raik, Jaan DDECS : 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 13-16, 2005, Sopron, Hungary : proceedings 2005 / p. 224-227 : ill

Handbook of testing electronic systems

Novak, Ondrej; Gramatova, Elena; **Ubar, Raimund-Johannes; Jutman, Artur; Raik, Jaan** 2005 https://www.ester.ee/record=b2102523*est

Hardware/Software co-design in practice : MEMOCODE'08 contest experience

Reinsalu, Uljana; Devadze, Sergei; Jutman, Artur; Tšertov, Anton; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 55-58 : ill

Health management for self-aware SoCs based on IEEE 1687 infrastructure

Shibin, Konstantin; Devadze, Sergei; Jutman, Artur; Grabmann, Martin; Pricken, Robin IEEE Design & Test 2017 / p. 27-35 : ill <https://doi.org/10.1109/MDAT.2017.2750902> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Hierarchical design error diagnosis in combinational circuits by stuck-at fault test patterns

Ubar, Raimund-Johannes; Jutman, Artur Proceedings of the 6th International Conference on Mixed Design of Integrated Circuits and Systems : MIXDES'99 : Krakow, Poland, 17-19 June 1999 1999 / p. 437-442 : ill <https://www.sciencedirect.com/science/article/pii/S0026271499002036>

HLS-based optimization of tau triggering algorithm for LHC: a case study

Cherezova, Natalia; Mihhailov, Dmitri; Devadze, Sergei; Jutman, Artur 2022 18th Biennial Baltic Electronics Conference (BEC) 2022 / 6 p. : ill <https://doi.org/10.1109/BEC56180.2022.9935599>

IEEE 1687 compliant ecosystem for embedded instrumentation access and in-field health monitoring

Tšertov, Anton; Jutman, Artur; Shibin, Konstantin; **Devadze, Sergei** IEEE AUTOTESTCON 2018 : National Harbor, September 17-20, 2018 : proceedings 2018 / 9 p.: ill <https://doi.org/10.1109/AUTEST.2018.8532559>

IEEE European Test Symposium (ETS)

Eggersgluss, Stephan; Hamdioui, Said; **Jutman, Artur;** Michael, Maria K.; **Raik, Jaan** 2019 IEEE International Test Conference (ITC) 2019 / 4 p <https://doi.org/10.1109/ITC44170.2019.9000148> [Conference proceeding at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

IEEE P1687 IJTAG demonstrator on FPGA

Shibin, Konstantin; Aleksejev, Igor; Jutman, Artur; Devadze, Sergei DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p. : ill https://www.academia.edu/22101517/IEEE_P1687_IJTAG_demonstrator_on_FPGA

Improving the efficiency of timing simulation in digital circuits by using structurally synthesized BDDs

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. IEEE Norchip Conference 2000 / p. 254-261

Increasing the speed of delay simulation in digital circuits

Ubar, Raimund-Johannes; Jutman, Artur The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 31-34 : ill

In-system programming of non-volatile memories on microprocessor-centric boards

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom International journal of microelectronics and computer science 2014 / p. 25-34 : ill

Internet-based software for teaching test of digital circuits

Ubar, Raimund-Johannes; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Evertson, Teet; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 4th European Workshop on Microelectronics Education : EWME 2002, Spain, May 23-24, 2002 2002 / p. 317-320 : ill <https://ieeexplore.ieee.org/document/1003344>

Invited paper: System-Wide Fault Management based on IEEE P1687 IJTAG

Jutman, Artur; Devadze, Sergei; Aleksejev, Jevgeni 6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC) : 20-22 June 2011, Montpellier, France 2011 / [4] p.: ill <https://ieeexplore.ieee.org/document/5981520>

Java applets support for an asynchronous-mode learning of digital design and test

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich ITHET 2003 proceedings : 4th International Conference on Information Technology Based Higher Education and Training : July 7-9, 2003, Marrakech, Morocco 2003 / p. 397-401 : ill <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=92f0b0e5011a2192d5a1b98baa751cb8cd2f7ff3>

Java technology based training system for teaching digital design and test

Devadze, Sergei; Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 283-286 : ill

Keynote: cost-efficient reliability for Edge-AI chips

Jenihhin, Maksim; Taheri, Mahdi; Cherezova, Natalia; Ahmadilivani, Mohammad Hasan; Selg, Hardi; Jutman, Artur; Shibin, Konstantin; Tsertov, Anton; Devadze, Sergei; Kodamanchili, Rama Mounika; Rafiq, Ahsan; Raik, Jaan; Daneshtalab, Masoud 2024 IEEE 25th Latin American Test Symposium (LATS) 2024 / 2 p <https://doi.org/10.1109/LATS62223.2024.10534610> [Article at Scopus](#)

Laboratory training for teaching design and test of digital circuits

Jutman, Artur; Ubar, Raimund-Johannes Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 521-524 : ill <https://pld.ttu.ee/~artur/papers/TestLabs-MIXDES01.pdf>

Learning digital test and diagnostics via internet

Ubar, Raimund-Johannes; Jutman, Artur; Kruus, Margus; Orasson, Elmet; Devadze, Sergei; Wuttke, Heinz-Dietrich International journal of online engineering 2007 / 1, [9] p. : ill https://www.db-thueringen.de/servlets/MCRFileNodeServlet/dbt_derivate_00032681/iJOE_1681-1221_03_2007_1_361.pdf

Learning digital test and diagnostics via internet [Electronic resource]

Ubar, Raimund-Johannes; Jutman, Artur; Kruus, Margus; Orasson, Elmet; Devadze, Sergei; Wuttke, Heinz-Dietrich International journal of computing & information sciences 2006 / 2, p. 86-96 : ill

LFSR polynomial and seed selection using genetic algorithm

Aleksejev, E.; Jutman, Artur; Ubar, Raimund-Johannes BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 179-182 : ill

Maagiline miljonipiiir on peagi ületatud : [2003. a. ületab TTÜ Arengufondi ja Vilistlaskogu stipendiumide kogusumma 1 miljoni : stipendiumitunnistuste pidulikust kätteandmisest 7. nov. Tallinna Raekoja rohkem kui 30-le TTÜ stipendiaadile, ka vastavad küsimustele: Gunnar Okk, Artur Jutman ja Toomas Luman]

Ummelas, Mart; Okk, Gunnar; Jutman, Artur; Luman, Toomas Mente et Manu 2002 / lk. 1 https://www.ester.ee/record=b1242496*est

Marginal PCB assembly defect detection on DDR3/4 memory bus

Odintsov, Sergei; Jutman, Artur; Devadze, Sergei 2017 IEEE International Test Conference (ITC 2017) : Forth Worth, Texas, USA, 31 October - 2 November 2017 2017 / p. 238-247 : ill <https://doi.org/10.1109/TEST.2017.8242070> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

A method for crosstalk fault detection in on-chip buses

Bengtsson, Tomas; Jutman, Artur; Ubar, Raimund-Johannes; Kumar, Shashi Norchip : proceedings : Oulu, Finland, 21-22 November 2005 2005 / p. 285-288 : ill <https://doi.org/10.1109/NORCHIP.2005.1597045>

Microprocessor modeling for board level test access automation

Devadze, Sergei; Jutman, Artur; Tsertov, Anton; Ubar, Raimund-Johannes Proceedings of 10th IEEE Workshop on RTL and High Level Testing : Hong Kong, November 27-28, 2009 2009 / ? p

Microprocessor-based system test using debug interface

Devadze, Sergei; Jutman, Artur; Tsertov, Anton; Istenberg, Martin; Ubar, Raimund-Johannes 26th Norchip Conference : Tallinn, Estonia, 17-18 November 2008 : formal proceedings 2008 / p. 98-101 : ill <http://dx.doi.org/10.1109/NORCHIP.2008.4738291>

Modeling microprocessor faults on high-level decision diagrams [Electronic resource]

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim; Istenberg, Martin; Wuttke, Heinz-Dietrich DSN 2008 : supplemental : 2008 IEEE International Conference on Dependable Systems & Networks With FTCS & DCC (DSN) : June 24-27, 2008, Anchorage, Alaska 2008 / p. C17-C22 : ill. [CD-ROM] [https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08\(LAAS\)_files/Slides/WDSN08S-04-Ubar.pdf](https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08(LAAS)_files/Slides/WDSN08S-04-Ubar.pdf)

New built-in self-test scheme for SoC interconnect

Jutman, Artur; Ubar, Raimund-Johannes; Raik, Jaan The 9th World Multi-Conference on Systemics, Cybernetics and Informatics : WMSCI 2005 : July 10-13, 2005, Orlando, Florida, USA. Vol. IV 2005 / p. 19-24 : ill
https://www.researchgate.net/publication/237375234_New_Built-In_Self-Test_Scheme_for_SoC_Interconnect

A new FPGA-based detection method for spurious variations in PCBA power distribution network

Odintsov, Sergei; Bozzoli, Ludovica; De Sio, Corrado; Sterpone, Luca; Jutman, Artur 2019 22nd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Cluj-Napoca, Romania : proceedings 2019 / 6 p. : ill
<https://doi.org/10.1109/DDECS.2019.8724662>

A novel artificial neural networks based automatic adaptive fault detection technique for analog circuits

Petlenkov, Eduard; Jutman, Artur; Nõmm, Sven; Ubar, Raimund-Johannes BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 167-170 : ill

Off-line testing of crosstalk induced glitch faults in NoC Interconnects

Bengtsson, Tomas; Kumar, Shashi; Jutman, Artur; Ubar, Raimund-Johannes Proceedings [of] 24th IEEE Norchip Conference : Linköping, Sweden, 20-21 November 2006 2006 / p. 221-225 : ill <http://dx.doi.org/10.1109/NORCHP.2006.329215>

Off-line testing of delay faults in NoC interconnects

Bengtsson, Tomas; Jutman, Artur; Kumar, Shashi; Peng, Zebo; Ubar, Raimund-Johannes 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 677-680 : ill <http://dx.doi.org/10.1109/DSD.2006.72>

On coverage of timing related faults at board level

Jutman, Artur; Aleksejev, Igor; Devadze, Sergei 2016 21st IEEE European Test Symposium (ETS) : May 23rd-26th 2016, Amsterdam, The Netherlands : proceedings 2016 / [2] p. : ill <https://doi.org/10.1109/ETS.2016.7519295>

On efficient logic-level simulation of digital circuits represented by the SSBDD model

Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 621-624 : ill <https://ieeexplore.ieee.org/document/1003334>

On in-system programming of non-volatile memories

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom International journal of microelectronics and computer science 2013 / p. 72-78 : ill

On in-system programming of non-volatile memories

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2013, Gdynia, Poland, June 20-22, 2013 2013 / p. 408-413 : ill

On LFSR polynomial calculation for test time reduction

Jutman, Artur Computer Science Meets Automation : 10-13 September 2007 : proceedings. Volume II 2007 / p. 153-158 : ill
https://www.db-thueringen.de/receive/dbt_mods_00008867

On SSBDD model size & complexity

Jutman, Artur ECS'03 : proceedings of the 4th Electronic Circuits and Systems Conference : September 11-12, 2003, Bratislava, Slovakia 2003 / p. 17-22 https://pld.ttu.ee/~artur/papers/SSBDD_Model_Size-ECS03.pdf

On-chip sensors data collection and analysis for SoC health management

Shibin, Konstantin; Jenihhin, Maksim; Jutman, Artur; Devadze, Sergei; Tsertov, Anton 2023 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2023 / 6 p <https://doi.org/10.1109/DFT59622.2023.10313562>

On-line fault classification and handling in IEEE1687 based fault management system for complex SoCs

Shibin, Konstantin; Devadze, Sergei; Jutman, Artur LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguaçu, Brazil, 6th-9th April 2016 2016 / p. 69-74 : ill <https://doi.org/10.1109/LATW.2016.7483342>

Open-source JTAG simulator bundle for labs

Shibin, Konstantin; Devadze, Sergei; Rosin, Vjatšeslav; Jutman, Artur; Ubar, Raimund-Johannes International journal of electronics and telecommunications 2012 / p. 233-239 : ill <https://journals.pan.pl/Content/87192/PDF/32.pdf>

Optimization of boundary scan tests using FPGA-based efficient scan architectures

Aleksejev, Igor; Devadze, Sergei; Jutman, Artur; Shibin, Konstantin Journal of electronic testing : theory and applications (JETTA) 2016 / p. 245-255 : ill <https://doi.org/10.1007/s10836-016-5588-y> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Optimization of structurally synthesized BDDs

Ubar, Raimund-Johannes; Vassiljeva, T.; **Raik, Jaan; Jutman, Artur;** Tombak, Mati; Peder, Ahti Proceedings of the Fourth IASTED International Conference on Modelling, Simulation, and Optimization : August 17-19, 2004, Kawai, Hawaii, USA 2004 / p. 234-240 : ill https://www.academia.edu/22101496/Optimization_of_structurally_synthesized_BDDs

Overview of e-learning environment for web-based study of testing and diagnostics of digital systems

Jutman, Artur; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 5th European Workshop on Microelectronics Education, held in Lausanne, Switzerland, April 15-16, 2004 2004 / p. 253-258 : ill https://link.springer.com/chapter/10.1007/978-1-4020-2651-5_41

Overview of e-learning environment for web-based study of testing and diagnostics of digital systems

Jutman, Artur; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 5th European Workshop on Microelectronics Education - EWME 2004, Lausanne, 2004 2004 / p. 173-176 https://link.springer.com/chapter/10.1007/978-1-4020-2651-5_41

Parallel exact critical path tracing fault simulation with reduced memory requirements

Devadze, Sergei; Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur 4th International Conference on Design and Technology of Integrated Systems in Nanoscale Era : DTIS'09 : Cairo, Egypt, April 6-9, 2009 2009 / p. 155-160 : ill <https://ieeexplore.ieee.org/document/4938046>

Parallel fault backtracing for calculation of fault coverage

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur 43rd International Conference on Microelectronics, Devices and Materials and the Workshop on Electronic Testing : September 12. - September 14.2007, Bled, Slovenia : MIDEM conference 2007 proceedings 2007 / p. 165-170 : ill https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel fault backtracing for calculation of fault coverage

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur Proceedings of the ASP-DAC 2008 : [13th] Asia and South Pacific Design Automation Conference 2008 : January 21-24, 2008, COEX, Seoul, Korea 2008 / p. 667-672 : ill https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel X-fault simulation with critical path tracing technique [Electronic resource]

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur DATE 10 : Design, Automation & Test in Europe : Dresden, Germany, 8-12 March, 2010 2010 / p. 879-884 [CD-ROM] https://www.researchgate.net/publication/221341788_Parallel_X-fault_simulation_with_critical_path_tracing_technique

Post-silicon validation of IEEE 1687 reconfigurable scan networks

Damljanovic, Aleksa; Jutman, Artur; Squillero, Giovanni; Tšertov, Anton 2019 IEEE European Test Symposium (ETS) : proceedings 2019 / 6 p. : ill <https://doi.org/10.1109/ETS.2019.8791546>

Practical works for on-line teaching design and test of digital circuits

Jutman, Artur; Ubar, Raimund-Johannes; Hahanov, V.; Skvortsova, O. The 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS 2002 : September 15-18, 2002, Dubrovnik, Croatia. Volume III 2002 / p. 1223-1226 : ill <http://dx.doi.org/10.1109/ICECS.2002.1046474>

Reliable health monitoring and fault management infrastructure based on embedded instrumentation and IEEE 1687

Jutman, Artur; Shibin, Konstantin; Devadze, Sergei IEEE AUTOTESTCON 2016 : Anaheim, California, USA, September 12-15, 2016 : proceedings 2016 / p. 240-249 : ill <https://doi.org/10.1109/AUTEST.2016.7589605>

Research environment for teaching digital test

Ivask, Eero; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Synergies between Information and Automation : 49. Internationales Wissenschaftliches Kolloquium, 27.-30.9.2004, Technische Universität Ilmenau, Germany. Volume 2 2004 / p. 468-473 : ill https://pld.ttu.ee/dildis/publications/IWK'2004_res_inv.pdf

Research in digital design and test at Tallinn University of Technology

Ubar, Raimund-Johannes; Jervan, Gert; Jutman, Artur; Raik, Jaan; Ellervee, Peeter; Kruus, Margus Radioelectronics & informatics 2008 / p. 4-12 : ill <http://www.ewdtest.com/ri/%E2%84%96-1-40-january-march-2008/>

Research on digital system design and test at Tallinn University of Technology

Ubar, Raimund-Johannes; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert; Jutman, Artur; Kruus, Margus; Raik, Jaan Research in Estonia : present and future 2011 / p. 184-205 : ill

Reseeding using compaction of pre-generated LFSR sequences

Jutman, Artur; Alekseev, Igor; Raik, Jaan; Ubar, Raimund-Johannes ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : 31st August to 3rd September 2008, Malta : conference guide 2008 / p. 215

Reseeding using compaction of pre-generated LFSR sub-sequences

Jutman, Artur; Alekseev, Igor; Raik, Jaan; Ubar, Raimund-Johannes ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : Malta 2008 / p. 1290-1295 : ill <http://dx.doi.org/10.1109/ICECS.2008.4675096>

Re-using chip level DFT at board level

Gu, Xinli; **Jutman, Artur** Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th–June 1st, 2012, Annecy, France 2012 / 1 p https://www.academia.edu/25351525/Re_using_chip_level_DFT_at_board_level

Run-time reconfigurable instruments for advanced board-level testing

Aleksejev, Igor; Jutman, Artur; Devadze, Sergei IEEE AUTOTESTCON 2016 : Anaheim, California, USA, September 12-15, 2016 : proceedings 2016 / p. 385-392 : ill <https://doi.org/10.1109/AUTEST.2016.7589627>

Run-time reconfigurable instruments for advanced board-level testing

Aleksejev, Igor; Jutman, Artur; Devadze, Sergei IEEE instrumentation & measurement magazine 2017 / p. 23-30 : ill <https://doi.org/10.1109/MIM.2017.8006390>

Selected issues of modeling, verification and testing of digital systems

Jutman, Artur 2004 https://www.ester.ee/record=b1989760*est

Sequential test set compaction in LFSR reseeding

Jutman, Artur; Aleksejev, Igor; Raik, Jaan Design and test technology for dependable systems-on-chip 2011 / p. 476-493 : ill <https://ieeexplore.ieee.org/document/4738292>

Shift register based TPG for at-speed interconnect BIST

Jutman, Artur MIEL 2004 : 24th International Conference on Microelectronics : Niš, Serbia and Montenegro, 16-19 May 2004 : proceedings. Volume 2 2004 / p. 751-754 : ill <https://ieeexplore.ieee.org/document/1314941?signout=success>

Simulation-based equivalence checking between IEEE 1687 ICL and RTL

Damljanovic, Aleksa; **Jutman, Artur**; Portolan, Michele; Tšertov, Anton 2019 IEEE International Test Conference (ITC) 2019 / paper. 7.3, 8 p. : ill <https://doi.org/10.1109/ITC44170.2019.9000181>

SoC and board modeling for processor-centric board testing

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 14th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2011 : 31 August - 2 September 2011, Oulu, Finland : proceedings 2011 / p. 575-582 : ill <https://ieeexplore.ieee.org/document/6037463>

SSBDD model : advantageous properties and efficient simulation algorithms

Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes ETW'02 : 7th IEEE European Test Workshop, Gorfou Greece, May 26-29, 2002 : informal digest 2002 / p. 345-346 : ill

SSBDDs : advantageous model and efficient algorithms for digital circuit modeling, simulation & test

Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes 5th International Workshop on Boolean Problems : September 19-20, 2002, Freiberg (Sachsen) : proceedings 2002 / p. 157-166 : ill

Structural decision diagrams in digital test : theory and applications

Ubar, Raimund-Johannes; Raik, Jaan; Jenihhin, Maksim; Jutman, Artur 2024 <https://doi.org/10.1007/978-3-031-44734-1> https://www.ester.ee/record=b5734441*est

Structural fault collapsing by superposition of BDDs for test generation in digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur Proceedings of the Eleventh International Symposium on Quality Electronic Design ISQED 2010 : March 22-24, 2010 San Jose, California USA 2010 / p. 250-257 : ill <https://ieeexplore.ieee.org/document/5450451>

Structurally synthesized binary decision diagrams

Jutman, Artur; Peder, Ahti; Raik, Jaan; Tombak, Mati; Ubar, Raimund-Johannes Boolean Problems : 6th International Workshop : September 23-24, 2004, Freiberg 2004 / p. 271-278 : ill

Structurally synthesized multiple input BDDs for simulation of digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunisia, 13-19 December, 2009 2009 / p. 451-454 : ill <http://dx.doi.org/10.1109/ICECS.2009.5410895>

Structurally synthesized multiple input BDDs for speeding up logic-level simulation of digital circuits

Mironov, Dmitri; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur 13th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2010 : Lille, France, 1-3 September 2010 : proceedings 2010 / p. 658-663 : ill <https://ieeexplore.ieee.org/document/5615526>

A suite of IEEE 1687 benchmark networks

Tšertov, Anton; Jutman, Artur; Devadze, Sergei 2016 IEEE International Test Conference (ITC) : proceedings 2016 / art. 6.1, p. 1-10 : ill <https://doi.org/10.1109/TEST.2016.7805840>

Synchronization, calibration and triggering of IEEE 1687 embedded instruments

Jutman, Artur; Devadze, Sergei; Shibin, Konstantin The Seventeenth Workshop on RTL and High Level Testing (WRTL'16) : November 24-25, 2016, Aki Grand Hotel, Hiroshima, Japan 2016 / [6] p

A system for teaching basic and advanced topics of IEEE 1149.1 boundary scan standard (extended abstract)

Jutman, Artur; Rosin, Vjatšeslav; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of 16th EAEEIE Conference on Innovation in Education for Electrical and Information Engineering (EIE) : Lappeenranta, Finland, 6th-8th June 2005 2005 / [2] p. : ill

System modeling for processor-centric test automation = Süsteemide modelleerimine protsessorikesksete testprogrammide sünteesi automatiseerimiseks

Tšertov, Anton 2012 https://www.ester.ee/record=b2751131*est

System-wide fault management based on IEEE P1687 JTAG

Shibin, Konstantin; Jutman, Artur; Devadze, Sergei Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kuuenda aastakonverentsi artiklite kogumik : 3.-5. oktoobril 2012, Laulasmaa 2012 / p. 81-84 : ill

Teaching digital RT-level self-test using a Java applet

Devadze, Sergei; Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 2002 / p. 322-328 : ill

Teaching digital test with BIST analyzer

Jutman, Artur; Tšertov, Anton; Tšepurov, Anton; Aleksejev, Igor; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 123-128 : ill
<http://dx.doi.org/10.1109/EAEEIE.2008.4610171>

Test methods for crosstalk-induced delay and glitch faults in network-on-chip interconnects implementing asynchronous communication protocols

Bengtsson, Tomas; Kumar, Shashi; Ubar, Raimund-Johannes; Jutman, Artur; Peng, Zebo IET computers and digital techniques 2008 / 6, p. 445-460 https://www.diva-portal.org/smash/record.jsf?dswid=5073&aq2=%5B%5B%5D%5D&c=39&af=%5B%5D&searchType=SIMPLE&sortOrder2=title_sort_asc&language=en&pid=diva2%3A290043&aq=%5B%5B%7B%22personId%22%3A%22authority-person%3A23389%22%7D%5D%5D&sf=all&aqe=%5B%5D&sortOrder=author_sort_asc&onlyFullText=false&noOfRows=50

Testing beyond the SoCs in a lego style

Tšertov, Anton; Jutman, Artur; Devadze, Sergei Proceedings of IEEE East-West Design & Test Symposium (EWDTS'10) : St. Petersburg, Russia, September 17-20, 2010 2010 / p. 334-338 : ill <https://ieeexplore.ieee.org/document/5742052>

Testing tools

Jutman, Artur Handbook of testing electronic systems 2005 / p. 361-365 : ill

Testing tools for training and education

Balaž, M.; Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 12th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2005 : Krakow, Poland, 22-25 June, 2005. Vol. 1 of 2 2005 / p. 671-676 : ill

The synthesis level in Bloom's taxonomy - a nightmare for an LMS

Wuttke, Heinz-Dietrich; Ubar, Raimund-Johannes; Henke, Karsten; Jutman, Artur 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 199-204 : ill <http://dx.doi.org/10.1109/EAEEIE.2008.4610186>

Timing simulation of digital circuits with binary decision diagrams

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. Design, Automation and Test in Europe : Conference and Exhibition 2001 : Munich, Germany, March 13-16, 2001 : proceedings 2001 / p. 460-466 : ill <https://ieeexplore.ieee.org/document/915063>

Towards artificial intelligence based automatic adaptive response analyzer for high frequency analog BIST

Petlenkov, Eduard; Jutman, Artur; Nõmm, Sven; Ubar, Raimund-Johannes CIMSA 2008 : IEEE International Conference on Computational Intelligence for Measurement Systems and Applications : Istanbul, Turkey, July 14-16, 2008 2008 / p. 99-104 : ill
<https://ieeexplore.ieee.org/document/4595841>

Trainer 1149 : a boundary scan simulation bundle with hardware support for labs

Shibin, Konstantin; Jutman, Artur Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 135-138 : ill

Trainer 1149: a boundary scan simulation bundle for labs

Jutman, Artur; Ubar, Raimund-Johannes; Devadze, Sergei; Shibin, Konstantin; Rosin, Vjatšeslav MIXDES 2011 : 18th International Conference "Mixed Design of Integrated Circuits and Systems" : June 16-18, 2011, Gliwice, Poland 2011 / p. 520-525

Turbo tester - diagnostic package for research and training

Aarna, Margit; Ivask, Eero; Jutman, Artur; Orasson, Elmet; Raik, Jaan; Ubar, Raimund-Johannes; Vislogubov, Vladislav; Wuttke, Heinz-Dietrich Radioelectronics and informatics 2003 / p. 69-73 : ill

Turning JTAG inside out for fast extended test access

Devadze, Sergei; Jutman, Artur; Aleksejev, Igor; Ubar, Raimund-Johannes 10th IEEE Latin American Test Workshop : 2-5 March 2009, Brazil 2009 / [6] p. : ill <https://ieeexplore.ieee.org/document/4813799>

Ultra fast parallel fault analysis on structurally synthesized BDDs

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 131-136 : ill <http://dx.doi.org/10.1109/ETS.2007.43>

Understanding boundary scan test with Trainer 1149

Jutman, Artur; Devadze, Sergei; Shibin, Konstantin; Rosin, Vjatšeslav; **Ubar, Raimund-Johannes** 22nd EAEEIE annual conference : June, 13-15, 2011, Maribor, Slovenia : conference book 2011 / p. 21-22 <https://ieeexplore.ieee.org/document/6165727>

Understanding fault-tolerance vulnerabilities in advanced SoC FPGAs for critical applications

Cherezova, Natalia; Shibin, Konstantin; Jenihhin, Maksim; Jutman, Artur Microelectronics reliability 2023 / art. 115010, 10 p. : ill <https://doi.org/10.1016/j.microrel.2023.115010> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Ways for board and system test to benefit from FPGA embedded instrumentation

Ehrenberg, Heiko; **Odintsov, Sergei; Devadze, Sergei; Jutman, Artur; Aleksejev, Igor;** Wenzel, Thomas 2019 IEEE AUTOTESTCON 2019 / 10 p : ill <https://doi.org/10.1109/AUTOTESTCON43700.2019.8961057>

Web based tools for synthesis and testing of digital devices

Devadze, Sergei; Jutman, Artur; Kruus, Margus; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes Proceedings of the International Conference on Computer Systems and Technologies (e-Learning) : CompSysTech'2002, Sofia, Bulgaria, 20-21 June 2002 / p. 1.9-1 - 1.9-6 : ill https://www.researchgate.net/publication/250738271_Web_Based_Tools_for_Synthesis_and_Testing_of_Digital_Devices

Web-based applet for teaching boundary scan standard IEEE 1149.1

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes Proceedings of the 10th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2003 : Lodz, Poland, 26-28 June 2003 2003 / p. 584-589 : ill <https://www.semanticscholar.org/paper/WEB-BASED-APPLET-FOR-TEACHING-BOUNDARY-SCAN-IEEE-.J.-Utlman/3bd1b47848612e44772b4c84a2913c419de940fa>

Web-based framework for distributed remote laboratory in the field of digital system test

Ivask, Eero; Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 182-187 : ill <http://dx.doi.org/10.1109/EAEEIE.2008.4610183>

Web-based software package for e-learning and research training in digital system design

Jutman, Artur; Kruus, Margus; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Информационные технологии в науке, образовании, телекоммуникации и бизнесе : Материалы XXXII Международной конференции IT+SE'2005 : Украина, Крым, Ялта-Гурзуф, 19-28 мая 2005 г 2005 / [2] p

Web-based training system for teaching basics of RT-level digital design, test, and design for test [Electronic resource]

Devadze, Sergei; Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes 9th International Conference MIXDES 2002 : Mixed Design of Integrated Circuits and Systems, Wroclaw, Poland, 20-22 June 2002 2002 / [6] p. : ill. [CD-ROM]

Web-based training system for teaching principles of boundary scan technique

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes Proceedings of the 14th EAEEIE Annual International Conference on Innovation in Education for Electrical and Information Engineering (EIE) : Gdansk, Poland, 2003 2003 / p. 1-6 : ill

Virtual reconfigurable scan-chains on FPGAs for optimized board test

Aleksejev, Igor; Jutman, Artur; Devadze, Sergei; Shibin, Konstantin 16th Latin American Test Symposium (LATS 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2015.7102411>