Hardware trojan insertion in finalized layouts : from methodology to a silicon demonstration
Perez, Tiago Diadami; **Pagliarini, Samuel Nascimento** IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2023 / p. 2094-2107 https://doi.org/10.1109/TCAD.2022.3223846 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Interpretable quantitative description of the digital clock drawing test for Parkinson's disease modelling
Nõmm, Sven; **Mašarov, Ilja**; Toomela, Aaro; Medijainen, Kadri; Taba, Pille 15th International Conference on Control, Automation, Robotics and Vision (ICARCV 2018) : Singapore, November 18-21, 2018 2018 / p. 1839-1844 : ill
https://doi.org/10.1109/ICARCV.2018.8581074

Latch-Based logic locking
Sweeney, J.; Mohammed Zackriya, V.; **Pagliarini, Samuel Nascimento**; Pileggi, Larry Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust, HOST 2020 2020 / p. 132−141 : ill
https://doi.org/10.1109/HOST45689.2020.9300256

SCAAT: Secure cache alternative address table for mitigating cache logical side-channel attacks
Shalabi, Ameer; **Ghasempouri, Tara**; **Ellervee, Peeter**; **Raik, Jaan** 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / art, 20035366, p. 213−217 https://doi.org/10.1109/DSD51259.2020.00043