Design understanding : from logic to specification
Fey, Goerschwin; **Ghasempouri, Tara**; Jacobs, Swen; **Raik, Jaan** Proceedings of the 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 8-10, 2018, Verona, Italy 2018 / p. 172–175 : ill https://doi.org/10.1109/VLSI-SoC.2018.8644732

Engineering of an effective automatic dynamic assertion mining platform
Ghasempouri, Tara; Malburg, Jan; Danese, Alessandro; Pravadelli, Graziano; Fey, Goerschwin; **Raik, Jaan** VLSI-SoC 2019 : 27th IFIP/IEEE International Conference on Very Large Scale Integration : [proceedings] 2019 / p. 111-116 : ill https://doi.org/10.1109/VLSI-SoC.2019.8920331

Software-level TMR approach for on-board data processing in space applications
Janson, Karl; Treudler, Carl Johann; **Hollstein, Thomas**; **Raik, Jaan**; **Jenihhin, Maksim**; Fey, Goerschwin 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 147-152 : ill https://doi.org/10.1109/DDECS.2018.00033