

Address-based data processing over N-ary trees

Sklyarov, Valery; Skliarova, Iuliia; **Kruus, Margus; Mihhailov, Dmitri; Sudnitsõn, Aleksander** EuroCon 2013 : 01-04 July 2013, Zagreb, Croatia 2013 / p. 1790-1797 : ill

An external test approach for network-on-a-chip switches

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 185-190 : ill

An external test approach for network-on-a-chip switches

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes ATS '06 : Proceedings of the 15th Asian Test Symposium : November 20-23, 2006, Fukuoka, Japan 2006 / p. 437-442 : ill <http://dx.doi.org/10.1109/ATS.2006.23>

Analog design tools : n problems

Kukk, Vello BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 2 1994 / p. 375-384: ill https://www.ester.ee/record=b2150914*est

Analog integrated circuits and signal processing

Ellervee, Peeter; Jervan, Gert 2010

Analysis of a test method for delay faults in NoC interconnects

Bengtsson, Tomas; **Jutman, Artur; Kumar, Shashi; Ubar, Raimund-Johannes; Peng, Zebo** Proceedings of the IEEE East-West Design & Test Workshop (EWDWTW'06) : Sochi, Russia, September 15-19, 2006 2006 / p. 42-46 : ill

Analysis of defect tolerant crossbar network implementations

Leveugle, R.; Brahic, P. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 37-40: ill

Analyzing side-channel attack vulnerabilities at RTL

Lai, Xinhui; Jenihhin, Maksim 2023 IEEE 24th Latin American Test Symposium (LATS) 2023 / 2 p. : ill <https://doi.org/10.1109/LATS58125.2023.10154497>

Application specific true critical paths identification in sequential circuits

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan; Devadze, Sergei; Oyeniran, Adeboye Stephen 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 299-304 : ill <https://doi.org/10.1109/IOLTS.2019.8854442>

APRICOT : a framework for teaching digital systems verification

Raik, Jaan; Jenihhin, Maksim; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes 19th EAAEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 172-177 : ill <http://dx.doi.org/10.1109/EAAEIE.2008.4610181>

Architectural solutions for high-speed data processing demands of CERN LHC detectors with FPGA and high-level synthesis

Devadze, Sergei; Nielsen, Christine Elizabeth; Mihhailov, Dmitri; Ellervee, Peeter 2024 IEEE Nordic Circuits and Systems Conference (NorCAS) 2024 <https://doi.org/10.1109/NorCAS64408.2024.10752490> [Article at Scopus](#)

Area efficient design and implementation of a novel divider circuit block = Uudne efektiivne jagamistehte riistvaraline realiseerimine

Patankar, Udayan Sunil 2025 https://www.ester.ee/record=b5746970*est <https://digikogu.taltech.ee/et/Item/bada7a0d-f54f-48bb-844d-37e23ad8d029> <https://doi.org/10.23658/taltech.29/2025>

Areeba : an area efficient binary huff-curve architecture

Sajid, Asher; Rashid, Muhammad; Jamal, Sajjad Shaukat; **Imran, Malik; Alotaibi, Saud S.; Sinky, Mohammed H.** Electronics (Switzerland) 2021 / art. 1490 <https://doi.org/10.3390/electronics10121490> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Arvuti nõopaugus

Agur, Ustus Horisont 1976 / lk. 12-15 : ill https://www.ester.ee/record=b1072243*est <http://www.digar.ee/id/nlib-digar:291330>

Arvutiteadlased: USA kiibipiirang lõob Eesti digiarengul hinge kinni

novaator.err.ee 2025 [Arvutiteadlased: USA kiibipiirang lõob Eesti digiarengul hinge kinni](#)

ASIC for alcohol sensor

Kasemaa, Argo; Rang, Toomas BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 283-286: ill

ASIC prototyping for reprogrammable implementations of large ASICs

Krupnova, Helena ACM/SIGDA 4th International Symposium on FPGAs, Monterey, USA, February 11-13, 1996 : proceedings 1996

ASIC prototyping with area oriented mapping for ALTERA/FLEX devices

Krupnova, Helena Synthesis and System Integration of Mixed Technologies - SASMI'95, Nara, Japan, August 25-26, 1995 : proceedings 1996

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart 31st Norchip Conference : Vilnius, Lithuania, 11-12 November 2013 : conference program and papers 2013 / p. 1-6 : ill [USB]

Automated design error debug using high-level decision diagrams and mutation operators

Raik, Jaan; Repinski, Urmis; Tšepurov, Anton; Hantson, Hanno; Ubar, Raimund-Johannes; Jenihhin, Maksim

Microprocessors and microsystems 2013 / p. 505-513 : ill <https://doi.org/10.1016/j.micpro.2012.11.004> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Automated design error localization in RTL designs

Jenihhin, Maksim; Tšepurov, Anton; Tihomirov, Valentin; Raik, Jaan; Hantson, Hanno; Ubar, Raimund-Johannes;

Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich IEEE design & test of computers 2014 / p. 83-92 : ill

<https://doi.org/10.1109/MDAT.2013.2271420> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Automated identification of application-dependent safe faults in automotive systems-on-a-chips

Bagbaba, Ahmet Cagri; Augusto da Silva, Felipe; Sonza Reorda, Matteo; Hamdioui, Said; **Jenihhin, Maksim;** Sauer, Christian

Electronics 2022 / art. 319 <https://doi.org/10.3390/electronics11030319> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Automatic SoC level test path synthesis based on partial functional models

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 2011 Asian Test Symposium (ATS) : New Delhi,

India 2011 / p. 532-538 <https://ieeexplore.ieee.org/document/6114730>

Benchmarking advanced security closure of physical layouts

Eslami, Mohammad; Knechtel, Johann; Sinanoglu, Ozgur; Karri, Ramesh; **Pagliarini, Samuel Nascimento** ISPD '23 : proceedings

of the 2023 International Symposium on Physical Design 2023 / p. 256-264 <https://doi.org/10.1145/3569052.3578924>

<https://dl.acm.org/doi/pdf/10.1145/3569052.3578924>

Biotundlikud süsteemid molekulaarselt jäljendatud elektrit juhtivatest polümeeridest

Õpik, Andres; Reut, Jekaterina; Sõritski, Vitali; Tretjakov, Aleksei Tallinna Tehnikaülikooli aastaraamat 2012 2013 / lk. 40-44 : ill

BIST analyzer : a training platform for SoC testing [Electronic resource]

Jutman, Artur; Tšertov, Anton; Tšepurov, Anton; Aleksejev, Igor; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 37th

Annual Frontiers in Education Conference : Global Engineering : Knowledge Without Borders, Opportunities Without Passports :

Milwaukee, Wisconsin, October 10-13, 2007 2007 / p. S3H-8-S3H-13 : ill. [CD-ROM] <http://dx.doi.org/10.1109/FIE.2007.4418125>

CAC 2.0 : a corrupt and correct logic locking technique resilient to structural analysis attacks

Aksoy, Levent; Yasin, Muhammad; **Pagliarini, Samuel Nascimento** 2024 IEEE 25th Latin American Test Symposium (LATS) : 9-

12 April 2024 (2024) 2024 <https://doi.org/10.1109/LATS62223.2024.10534592> [Article at Scopus](#)

A CAD system for teaching digital test

Ubar, Raimund-Johannes; Ivask, Eero; Paomets, Priidu; **Raik, Jaan** BEC : Baltic Electronics Conference : proceedings of the 4th

Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 369-372: ill

Cal-Techist Pocketronicuni

Toomsalu, Arvo A & A 2005 / 4, lk. 9-12 https://artiklid.elnet.ee/record=b1018130*est

Capacitance measurement with MSP430 microcontrollers

Märtens, Olev; Pille, Siim; Reidla, Marko EDERC2014 : proceedings of the 6th European Embedded Design in Education and

Research Conference, 11-12 September 2014, Milan, Italy 2014 / p. 260-263 : ill

Capacitance-to-digital: A single chip detector for capillary electrophoresis

Drevinskas, Tomas; Kaljurand, Mihkel; Maruška, Audrius Electrophoresis 2014 / p. 2401-2407 : ill

<https://doi.org/10.1002/elps.201300468> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Chip-to-Chip authentication method based on SRAM PUF and public key cryptography

Karageorgos, Ioannis; Isgenc, Mehmet Meric; Pagliarini, Samuel Nascimento; Pileggi, Larry Journal of hardware and systems

security 2019 / p. 382-396 : ill <https://doi.org/10.1007/s41635-019-00080-y>

Circuit simulation program oriented physical modeling of integrated circuit elements

Rang, Toomas; Tarnay, K.; Szekely, V. Periodica polytechnica. Electrical engineering = Электротехника 1980 / p. 37-45
https://www.ester.ee/record=b1198855*est

Code coverage analysis for concurrent programming languages using high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes Proceedings of the 12th European Workshop on Dependable Computing : EWDC 2009 : Toulouse, France, May 14-15, 2009 2009 / [4] p. : ill
<https://hal.archives-ouvertes.fr/hal-00381559>

Combining symbolic techniques with topological approach in test generation

Ubar, Raimund-Johannes Proceedings of the 3rd Workshop on Mixed Design of Integrated Circuits and Systems, Lodz, May 1996 1996 / p. 377-382

A compact 16*16 CMOS cellular neural network chip

Paasio, Ari; Dawidziuk, Adam; Porra, Veikko BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 171-174: ill

Compact avalanche transistor model for circuit simulation of Bi and BiCMOS cells

Bubennikov, Alexander N.; Kobosev, Gennady; Kozuhov, D.; Uchenov, A. BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 2 1994 / p. 523-527: ill https://www.ester.ee/record=b2150914*est

Computational kernel extraction for synthesis of power-managed sequential components

Sudnitsõn, Aleksander Proceedings of the 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS'2002, Dubrovnik, Croatia 2002 / p. 749-752 <https://ieeexplore.ieee.org/abstract/document/1046277>

Computer scientists: Estonia's digital development held back by US chip limit

news.err.ee 2025 [Computer scientists: Estonia's digital development held back by US chip limit](#)

Construction of the tests of combinational circuit failures by analyzing the orthogonal disjunctive normal forms represented by the alternative graphs

Matrosova, A.Yu.; Pleshkov, A.G.; **Ubar, Raimund-Johannes** Automation and remote control 2005 / p. 313-327 : ill
<https://doi.org/10.1007/s10513-005-0054-9>

Decision diagrams - from a mathematical notion to engineering applications

Stankovic, Radomir S.; **Ubar, Raimund-Johannes**; Astola, Jaakko Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 281-301 : ill <http://dx.doi.org/10.2298/FUEE1103281S>

Defect-oriented test- and layout-generation for standard-cell ASIC designs

Sudbrock, Joachim; **Raik, Jaan; Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw; Pleskacz, Witold A. Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 79-82 : ill <https://ieeexplore.ieee.org/document/1559781>

Defect-oriented test generation using probabilistic estimation

Cibakova, Tatiana; Fischerova, Maria; Gramatova, Elena; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 131-136 : ill

DefSim - the defective IC

Pleskacz, Witold A.; **Jutman, Artur; Ubar, Raimund-Johannes; Devadze, Sergei** DATE 2007 : Design Automation and Test in Europe : Nice, France, April 16-20, 2007 2007 / p. s96 (2 p.)

DefSim: CMOS defects on chip for research and education

Pleskacz, Witold A.; Borejko, Tomasz; Walkanis, A.; Stopjakova, Viera; **Jutman, Artur; Ubar, Raimund-Johannes** 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 74-79 : ill

DefSim: measurement environment for CMOS defects

Borejko, Tomasz; **Jutman, Artur**; Pleskacz, Witold A.; **Ubar, Raimund-Johannes** 2006 25th International Conference on Microelectronics : Belgrade, Serbia and Montenegro, 14-17 May 2006 : proceedings. Volume 2 2006 / p. 679-682
<https://ieeexplore.ieee.org/document/1651048>

Delay testing of asynchronous NoC interconnects

Bengtsson, Tomas; **Jutman, Artur**; Kumar, Shashi; **Ubar, Raimund-Johannes** Proceedings of the 12th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2005 : Krakow, Poland, 22-25 June, 2005. Vol. 1 of 2 2005 / p. 419-424 : ill

Design and optimization of super-speed CMOS/CBiCMOS circuits based on TCAD and time-logical simulator

Bubennikov, Alexander; Blinnik, Semen B. BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 473-474: ill

Design and test technology for dependable systems-on-chip

2011 https://www.eester.ee/record=b4467408*est

Design methodology for fault-tolerant heterogeneous MPSoC under real-time constraints

Amin, Mohsin; Tagel, Mihkel; Jervan, Gert; Hollstein, Thomas 7th International Workshop on Reconfigurable and Communication-Centric Systems-on-Chip : July 9-11, 2012 : York, United Kingdom : proceedings 2012 / [6 p.] : ill
<https://ieeexplore.ieee.org/document/6322901>

Design of a generalized fractional-order PID controller using operational amplifiers

Gonzalez, Emmanuel A.; Alimisis, Vassilis; Psychalinos, Costas; **Tepljakov, Aleksei** 2018 25th IEEE International Conference on Electronics Circuits and Systems (ICECS), Bordeaux, France, December 9–12, 2018 2018 / p. 253-256 : ill
<http://dx.doi.org/10.1109/ICECS.2018.8617954>

Design space exploration and optimisation for NoC-based timing sensitive systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 177-180 : ill

Design space exploration and optimisation for NoC-based timing sensitive systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 117-120 : ill

Design-aid programs for LSI integrated circuits

Tarnay, K.; Szekeley, V.; Baji, P.; Farkas, G.; Masszi, F.; Kerecsen-Rencz, M. Проблемы моделирования и измерения в электронике 1986 / p. 3-11

Design-for-destability-based external test and diagnosis of mesh-like network- on-a-chips

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes IET computers and digital techniques 2009 / 5, p. 476-486 : ill
<http://dx.doi.org/10.1049/iet-cdt.2008.0096>

Determined-safe faults identification : a step towards ISO26262 hardware compliant designs

Augusto da Silva, Felipe; **Bagbaba, Ahmet Cagri**; Sartoni, Sandro; Cantoro, Riccardo; Sonza Reorda, Matteo; Hamdioui, Said; Sauer, Christian 2020 25th IEEE European Test Symposium (ETS) 2020 / 6 p. : ill <https://doi.org/10.1109/ETS48528.2020.9131568>

Diagnostic modeling of digital systems with low- and high-level decision diagrams

Ubar, Raimund-Johannes LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [1] p

Digitaalkiipide projekteerimine ja test : teadus, tehnoloogia või kunst

Raik, Jaan A & A 2005 / lk. 5-9

Digital hardware organization course for SoC program

Ellervee, Peeter; Tenhunen, Hannu 2001 International Conference on Microelectronic Systems Education : June 17-18, 2001, Las Vegas, Nevada, USA : proceedings 2001 / p. 26-27 <https://ieeexplore.ieee.org/document/932402>

Digital logic simulation with compressed BDDs

Ubar, Raimund-Johannes; Mironov, Dmitri; Devadze, Sergei; Raik, Jaan Proceedings : 2011 IEEE International Conference on Computer Science and Automation Engineering : June 10-12, 2011, Shanghai, China 2011 / p. 105-109 : ill
<https://ieeexplore.ieee.org/document/5952643>

Discrete gravitational search algorithm for solving finite state machine inference problem

Spitšakova, Margarita Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 63-66 : ill

Division Method And Circuit

Patankar, Udayan Sunil; Koel, Ants; Patankar, Sunil; Flores, Miguel E. 2022 <https://www.wipo.int>

Droonide lihtsus ja odavus võimaldab neid sõjas massiliselt kasutada [Võrguväljaanne]

Klementi, Joakim err.ee 2022 [Droonide lihtsus ja odavus võimaldab neid sõjas massiliselt kasutada](https://trialoog.taltech.ee/eesti-kiibikeskus-avas-kogukonnalehe-kiip-ee/)

Eesti kiibikeskus avas kogukonnalehe kiip.ee

Tambur, Silver Trialoog 2025 <https://trialoog.taltech.ee/eesti-kiibikeskus-avas-kogukonnalehe-kiip-ee/>

Eesti teadlased loodavad panna putukrobotile pähe tehisaru

Raik, Jaan novaator.err.ee 2024 [Eesti teadlased loodavad panna putukrobotile pähe tehisaru](#) [Эстонские ученые создают робота-насекомого с искусственным интеллектом](#)

Eesti teaduse nähtamatud hiiglased

Raik, Jaan Teadusmõte Eestis (X). Tehnikateadused. 3 : [artiklikogumik] 2019 / lk. 161-168 : ill., fot
https://www.ester.ee/record=b5208765*est

Eestisse luuakse kiibitehnoloogia kompetentsikeskus

Tambur, Silver Trialoog 2025 <https://trialoog.taltech.ee/eestisse-luuakse-kiibitehnoloogia-kompetentsikeskus/>

Elektroonika

Velmre, Enn TEA entsüklopeedia. 6. köide, eerika - faiaagid 2011 / lk. 199

Elliptic-curve crypto processor for RFID applications

Rashid, Muhammad; Jamal, Sajjad Shaukat; Khan, Sikandar Zulqarnain; Alharbi, Adel R.; Aljaedi, Amer; **Imran, Malik** Applied Sciences (Switzerland) 2021 / art. 7079 <https://doi.org/10.3390/app11157079> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Equivalent transformations of structurally synthesized BDDs and applications

Jürimägi, Lembit; Ubar, Raimund-Johannes; Viies, Vladimir 2019 8th Mediterranean Conference on Embedded Computing (MECO) 2019 / 6 p. : ill <https://doi.org/10.1109/MECO.2019.8760283>

Error sources in analog ASICs and ways for their minimization

Mihhailov, Juri International journal of engineering and applied sciences (EAAS) 2013 / p. 32-41 : ill

Esimene üldkasutatav mikrokontrollerkiip TMS 1000

Toomsalu, Arvo A & A 2008 / 2, lk. 9-16 : ill

European Test Symposium : ETS 2005 : 22-25 May 2005, Tallinn, Estonia : proceedings

Cantarella, JD 2005 https://www.ester.ee/record=b2300865*est

Evaluating architectural, redundancy, and implementation strategies for radiation hardening of FinFET integrated circuits

Pagliarini, Samuel Nascimento; Benites, Luis; Martins, Mayler; Rech, Paolo; Kastensmidt, Fernanda IEEE transactions on nuclear science 2021 / p. 1045-1053 <https://doi.org/10.1109/TNS.2021.3070643> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Evaluating NTT/INTT implementation styles for post-quantum cryptography

Imran, Malik; Khan, Safiullah; Khalid, Ayesha; Rafferty, Ciara; Ali Shah, Yasir; Pagliarini, Samuel; Rashid, Muhammad; O'Neill, Maire IEEE Embedded Systems Letters 2024 / p. 485 - 488 <https://doi.org/10.1109/LES.2024.3410516> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast test cost calculation for hybrid BIST in digital systems

Orasson, Elmet; Raidma, Rein; **Ubar, Raimund-Johannes;** Jervan, Gert; Peng, Zebo Euromicro Symposium on Digital Systems Design : [Architectures, Methods and Tools : DSD 2001] : September 4-6, 2001, Warsaw, Poland : proceedings 2001 / p. 318-325 : ill <https://www.semanticscholar.org/paper/Fast-test-cost-calculation-for-hybrid-BIST-in-Orasson-Raidma/5aafcd5a18c2aabf0ad20cac10af10727f3c58f>

Fault collapsing with linear complexity in digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS 2010) : 30 May - 2 June 2010, Paris, France 2010 / p. 653-656 : ill <https://ieeexplore.ieee.org/document/5537504>

Fault diagnosis in integrated circuits with BIST

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan; Evertson, Teet; Lensen, Harri 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 604-610 : ill <http://dx.doi.org/10.1109/DSD.2007.4341530>

Fault diagnosis in VLSI devices

Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 1995 / 1, p. 51-67

Fault effect reasoning in digital systems by topological view on low- and high-level decision diagrams

Ubar, Raimund-Johannes Вестник Томского государственного университета. Управление, вычислительная техника и информатика 2014 / p. 99-113 : ill http://journals.tsu.ru/informatics/&journal_page=archive&id=923&article_id=12107

Fault simulation with parallel critical path tracing for combinational circuits using structurally synthesized BDDs

Devadze, Sergei; Raik, Jaan; Jutman, Artur; Ubar, Raimund-Johannes 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 97-102 : ill

Faults and fault models for integrated circuits and systems [Electronic resource] : [slides]

Ubar, Raimund-Johannes Design and Test Technology for Dependable Hardware/Software Systems : DEDIS/DAAD Summer Academy : BTU Cottbus, Sept. 1st-12th, 2008 2008 / [64] p. : ill. [CD-ROM]

Finite state machines with datapath partitioning for low power synthesis

Sudnitsõn, Aleksander Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 163-168 : ill

Foreword to the 12th IEEE DDECS Symposium

Pliva, Zdenek; Manhaeve, Hans; Renovell, Michel; Novak, Ondrej; **Ubar, Raimund-Johannes**; Drabkova, Jindra Proceedings of the 2009 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 15-17, 2009, Liberec, Czech Republic 2009 / p. iii <http://dx.doi.org/10.1109/DDECS.2009.5012081>

From virtual characterization to test-chips : DFM analysis through pattern enumeration

Martins, Mayler G.A.; **Pagliarini, Samuel Nascimento**; Isgenc, Mehmet Meric; Pileggi, Larry IEEE transactions on computer-aided design of integrated circuits and systems 2020 / p. 520-532 <https://doi.org/10.1109/TCAD.2018.2889772>

Fully-fusible convolutional neural networks for end-to-end fused architecture with FPGA implementation

Dadras, Iman; Seydi, Sakineh; **Ahmadilivani, Mohammad Hasan; Raik, Jaan**; Salehi, Mostafa E. 2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2023 / 5 p. <https://doi.org/10.1109/ICECS58634.2023.10382831>

Functional partitioning for register transfer level low power synthesis

Sudnitsõn, Aleksander ECS'01 : proceedings of the 3rd Electronic Circuits and Systems Conference : September 5-7, 2001, Bratislava, Slovakia 2001 / p. 73-76 : ill

Gate-level modelling of NBTI-induced delays under process variations

Copetti, Thiago; Cardoso Medeiros, Guilherme; Bolzani Poehls, Leticia; Vargas, Fabian; **Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes** LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 75-80 : ill <http://dx.doi.org/10.1109/LATW.2016.7483343>

Generic interconnect BIST for Network-on-Chip

Jutman, Artur; Ubar, Raimund-Johannes; Raik, Jaan DDECS : 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 13-16, 2005, Sopron, Hungary : proceedings 2005 / p. 224-227 : ill

A global methodology for test program generation starting from high level specifications

Storojev, Sergei; Leveugle, Regis; Saucier, Gabriele BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 305-311 : ill https://www.ester.ee/record=b2150914*est

Hardware realization of lattice-based post-quantum cryptography = Võrel põhinev post-kvant-krüptograafia riistvaraline realiseatsioon

Imran, Malik 2023 https://www.ester.ee/record=b5571216*est <https://doi.org/10.23658/taltech.33/2023>
<https://digikogu.taltech.ee/et/Item/75aeb070-cb8b-4511-beaf-cbea3fca147d> https://www.ester.ee/record=b5571216*est

Hardware/software co-design for programmable systems-on-chip

Sklyarov, Valery; Skliarova, Ioulia; Silva, João; Rjabov, Artjom; **Sudnitsõn, Aleksander**; Cardoso, Cláudia 2014 http://www.ester.ee/record=b3087107*est

A healthier chip?

Ubar, Raimund-Johannes; Fridolin, Ivo; Meigas, Kalju; Min, Mart Public service review : European Union 2010 / p. 132-133 : ill

Hierarchical concurrent test generation for synchronous sequential circuits

Ubar, Raimund-Johannes; Brik, Marina Proceedings of the 7th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2000 : Gdynia, Poland, 15-17 June 2000 2000 / p. 533-538 : ill

High-level decision diagram based fault models for targeting FSMs

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 353-358 : ill <http://dx.doi.org/10.1109/DSD.2006.60>

High-Level Decision Diagram manipulations for code coverage analysis

Minakova, Karina; Reinsalu, Uljana; Tšepurov, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level decision diagrams based coverage metrics for verification and test

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes LATW 2009 : 10th IEEE Latin American Test Workshop : Buzios, Rio de Janeiro, Brazil, March 2-5, 2009 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2009.4813792>

High-level modeling and testing of multiple control faults in digital systems

Jasnetski, Artjom; Oyeniran, Adeboye Stephen; Tšertov, Anton; Schölzel, Mario; Ubar, Raimund-Johannes Formal proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 20-22, 2016, Košice, Slovakia 2016 / [6] p. : ill <http://dx.doi.org/10.1109/DDECS.2016.7482445>

High-speed SABER key encapsulation mechanism in 65nm CMOS

Imran, Malik; Almeida, Felipe; Basso, Andrea; Roy, Sujoy Sinha; Pagliarini, Samuel Nascimento Journal of cryptographic engineering 2023 / p. 461-471 : ill <https://doi.org/10.1007/s13389-023-00316-2> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Hiina võis sanktsioonide kiuste jõuda uue kiibitehnoloogiani [Võrguväljaanne]

Einama, Kaido Postimees 2022 [Hiina võis sanktsioonide kiuste jõuda uue kiibitehnoloogiani](#)

How to emulate Network-on-Chip?

Ellervee, Peeter; Jervan, Gert Proceedings of the IEEE East-West Design & Test Workshop (EWDWTW'06) : Sochi, Russia, September 15-19, 2006 / p. 282-286 : ill

Hybrid BIST optimization using reseeding and test set compaction

Jervan, Gert; Orasson, Elmet; Kruus, Helena; Ubar, Raimund-Johannes 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 596-603 : ill <http://dx.doi.org/10.1109/DSD.2007.4341529>

Hybrid protection of digital FIR filters

Aksoy, Levent; Nguyen, Quang-Linh; Almeida, Felipe; Raik, Jaan; Flottes, Marie-Lise; Dupuis, Sophie; Pagliarini, Samuel Nascimento IEEE transactions on Very Large Scale Integration (VLSI) Systems 2023 / p. 812-825 : ill <https://doi.org/10.1109/TVLSI.2023.3253641> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

PL új irányrat a bipoláris technikában I

Rang, Toomas Mérés és automatika: megjelenik a Méréstechnikai és Automatizálási Tudományos Egyesület Szerkesztésében 1979 / p. 191-195

PL, új irányrat a bipoláris technikában II

Rang, Toomas Mérés és automatika: megjelenik a Méréstechnikai és Automatizálási Tudományos Egyesület Szerkesztésében 1979 / p. 279-283

IEEE Norchip 2003. a. konverents

Ellervee, Peeter A & A 2004 / 1, lk. 48-49 https://artiklid.elnet.ee/record=b1015000*est

Impact of orientation on the bias of SRAM-based PUFs

Abideen, Zain Ul; Wang, Rui; Perez, Tiago Diadami; Schrijen, Geert-Jan; Pagliarini, Samuel Nascimento arXiv.org 2023 / 7 p. : ill <https://doi.org/10.48550/arXiv.2308.06730>

Impact of orientation on the bias of SRAM-based PUFs

Abideen, Zain Ul; Wang, Rui; Perez, Tiago Diadami; Schrijen, Geert-Jan; Pagliarini, Samuel Nascimento IEEE design & test 2024 / p. 14-20 <https://doi.org/10.1109/MDAT.2023.3322621> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

An improved test generation approach for sequential circuits using decision diagrams

Brik, Marina; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 155-158: ill

Improving the efficiency of timing simulation in digital circuits by using structurally synthesized BDDs

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. IEEE Norchip Conference 2000 / p. 254-261

Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005

2005 https://www.ester.ee/record=b2055139*est

Integraallülütus

Velmre, Enn TEA entsüklopeedia. 9. köide, indeen - Kallak 2012 / lk. 59-60 https://www.ester.ee/record=b2869027*est

Integraallülütuste hind

Toomsalu, Arvo A & A 2007 / 3, lk. 20-32 : ill

Integraallülituste pöördprojekteerimine

Toomsalu, Arvo A & A 1998 / 2, lk. 8-13

Integraalskeemide projekteerimine : metoodiline juhend

1988 https://www.ester.ee/record=b1239938*est

Integrált áramköri elemek fizikai modellezése aramkölanalizös program segítségével

Rang, Toomas; Tarnay, K.; Szekely, V. Híradástechnika = Journal on communications, computers, convergence, contents, companies 1980 / p. 322-326

Integrated analog front-end for ECG measurement

Siren, Harri; Kontra, Veli BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 203-204: ill

Integrated RF circuit solutions for radio communication systems

Halonen, Kari; Koli, Kimmo; Porra, Veikko BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 2 1994 / p. 473-478: ill https://www.ester.ee/record=b2150914*est

Intel 1103 - esimene DRAM-kiip

Toomsalu, Arvo A & A 2006 / 5, lk. 27-32 https://artiklid.elnet.ee/record=b1019636*est

Intel valmistub võitluseks

Toomsalu, Arvo Arvutustehnika ja Andmetöötlus 1995 / 2, lk. 9-13

Inteli P6 on valmis!

Toomsalu, Arvo Arvutustehnika ja Andmetöötlus 1995 / 6, lk. 2-9: ill

Interaction between point defects, extended defects and impurities in the Si-SiO₂ system during the process of its formation

Kropman, Daniel; Kärner, T.; Abru, Uno; Ugaste, Ülo; **Mellikov, Enn** Thin solid films 2004 / 1/2, p. 53-57 : ill <https://www.sciencedirect.com/science/article/abs/pii/S0921510704003459>

Interaction between point defects, extended defects and impurities in the Si-SiO₂ system during the process of its formation

Kropman, Daniel; Kärner, T.; Abru, Uno; Ugaste, Ülo; **Mellikov, Enn**; **Kauk, Marit** Materials science and engineering : B 2004 / p. 295-298 : ill <https://www.sciencedirect.com/science/article/abs/pii/S0921510704003459>

Jaan Raik : müütidest Eesti elektroonikatööstuse väljavaadete ümber

Raik, Jaan err.ee 2022 [Jaan Raik: müütidest Eesti elektroonikatööstuse väljavaadete ümber](#)

Jaan Raik: Computers must undergo a revolution in order to continue their rapid development

Raik, Jaan Estonian Centre of Excellence in ICT Research 2021 / p. 43-47 : ill <http://www.digar.ee/id/nlib-digar:634779>
https://www.ester.ee/record=b5456158*est

Jaan Raik: kiibikriis – kas maailmalõpp või Eesti võimalus? [Võrguväljaanne]

postimees.ee 2021 ["Jaan Raik: kiibikriis – kas maailmalõpp või Eesti võimalus?"](#)

Journal of signal processing systems for signal, image, and video technology. Implementation issues in system-on-chip

2017 <https://link.springer.com/journal/11265/87/3/page/1>

Juhuved lausintegraallülitustes

Toomsalu, Arvo A & A 2007 / 1, lk. 8-21

Kas tehisintellekt on väikeriigi demokraatia ja julgeoleku tugi või oht?

Vaaks, Eveliis Trialoog 2025 <https://trialoog.taltech.ee/kas-tehisintellekt-on-vaikeriigi-demokraatia-ja-julgeoleku-tugi-voi-oht/>

Kiibiargonaudid, nende kuldvillak ja sümplegaadid

Tammemäe, Kalle; **Ellervee, Peeter** Informaatika perspektiivsed suunad : Eesti Teaduste Akadeemia seminari materjalid : 29.11.2000 2000 / lk. 17-20 : ill

Kiibikeskus kui ellujäämisvõimalus

Vaaks, Eveliis Trialoog 2025 <https://trialoog.taltech.ee/kiibikeskus-kui-ellujaaamisvoimalus/>

Kiibikriis: kas maailmalõpp või Eesti võimalus?

Raik, Jaan Postimees 2022 / Lk. 12 <https://dea.digar.ee/article/postimees/2021/12/14/12.4>

Kiipidest on saanud julgeolekuküsimus – neid arendatakse nüüd ka Eestis

postimees.ee 2025 <https://tehnika.postimees.ee/8256776/kiipidest-on-saanud-julgeolekukusimus-neid-arendatakse-nuud-ka-eestis>

Kolm TalTechi teadlast siirduvad Stanfordi ülikooli uurimistööd tegema [Võrguväljaanne]

postimees.ee 2022 "[Kolm TalTechi teadlast siirduvad Stanfordi ülikooli uurimistööd tegema](#) "

Kuidas mõjutab kiipsüsteem elektroonika-alast kõrgharidust?

Ellervee, Peeter A & A 2002 / 1, lk. 50-52

Kuidas saada kiipsüsteemi disaineriks

Tammemäe, Kalle A & A 2001 / 1, lk. 19-21

Kuidas suhtlevad kiibid e I2C ja SPI liidesed

Tammemäe, Kalle Arvutustehnika ja Andmetöötlus 1994 / 6, lk. 2-5 ; 7/8, lk. 2-4 ; 9, lk. 2-5 : ill

Kuidas testida arvutivõrku ränikiibil

Raik, Jaan; Govind, Vineeth A & A 2010 / 4, lk. 35-37 https://artiklid.elnet.ee/record=b2286479*est

Latch-Based logic locking

Sweeney, J.; Mohammed Zackriya, V.; **Paglierini, Samuel Nascimento**; Pileggi, Larry Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust, HOST 2020 2020 / p. 132–141 : ill
<https://doi.org/10.1109/HOST45689.2020.9300256>

Layout to logic defect analysis for hierarchical test generation

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Pleskacz, Witold A.; Rakowski, Michal Proceedings of the 2007 IEEE Workshop on Design and Diagnostic Circuits and Systems : April 11-13, 2007, Krakow, Poland 2007 / p. 35-40 : ill
<http://dx.doi.org/10.1109/DDECS.2007.4295251>

Lightweight monitoring scheme for flooding DoS Attack detection in multi-tenant MPSoCs

Chaves Arroyave, Cesar Giovanni; Sepulveda, Johanna; **Hollstein, Thomas** 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea May 22-28, 2021 : proceedings 2021 / 5 p <https://doi.org/10.1109/ISCAS51556.2021.9401153>
[Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Logic IP for low-cost IC design in advanced CMOS nodes

Isgenc, Mehmet Meric; Martins, Mayler G.A.; Zackriya, V. Mohammed; **Paglierini, Samuel Nascimento**; Pileggi, Larry IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2020 / p. 585-595 <https://doi.org/10.1109/TVLSI.2019.2942825>

Logic simulation and fault collapsing with shared structurally synthesized BDDs

Mironov, Dmitri; Ubar, Raimund-Johannes; Raik, Jaan 2014 19th IEEE European Test Symposium (ETS) : May 26th-30th, 2014, Paderborn, Germany : proceedings 2014 / [2] p. : ill

Low power finite state machine synthesis

Fomina, Jelena 2005 https://www.ester.ee/record=b2097121*est

Low power synthesis based on information theoretic measures

Fomina, Jelena; Keevallik, Andres; Sudnitsõn, Aleksander 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings 2002 / p. 699-702 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1003354>

Low voltage integrated BiCMOS circuits for a 2 GHz transceiver

Porra, Veikko; Halonen, Kari; Koli, Kimmo; Pääkkönen, M.; Siilasto, S.; Tiiliharju, E.; Tolonen, P.; Wahlroos, T. BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 175-178: ill

Low-area boundary BIST architecture for mesh-like network-on-chip

Raik, Jaan; Govind, Vineeth Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia 2012 / p. 95-100 : ill

Lower bounds of the size of shared structurally synthesized BDDs

Ubar, Raimund-Johannes; Mironov, Dmitri Proceedings of the 2014 IEEE 17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 23-25, 2014, Warsaw, Poland 2014 / p. 77-82 : ill

Madalapingelised integraallülitused

Toomsalu, Arvo Arvutustehnika ja Andmetöötlus 1996 / 4, lk. 7-10; 5, lk. 9-14; 6, lk. 6-9: ill

Majandusele oluline kiibikeskus võib 1 miljoni pärast käest libiseda: MKM kahtleb, EISA on poolt

Puusild, Harro aripaev.ee 2024 [Majandusele oluline kiibikeskus võib 1 miljoni pärast käest libiseda: MKM kahtleb, EISA on poolt](#)

A method for crosstalk fault detection in on-chip buses

Bengtsson, Tomas; Jutman, Artur; Ubar, Raimund-Johannes; Kumar, Shashi Norchip : proceedings : Oulu, Finland, 21-22 November 2005 2005 / p. 285-288 : ill <https://doi.org/10.1109/NORCHIP.2005.1597045>

Methode et outil de prototypage des systemes integres sur FPGAs : [doktoriväitekirj]

Krupnova, Helena 1999

Methods to optimize functional safety assessment for automotive integrated circuits = Meetodid autotööstuse kiipide funktsionaalse ohutuse hindamise optimeerimiseks

Bagbaba, Ahmet Cagri 2022 <https://doi.org/10.23658/taltech.9/2022> <https://digikogu.taltech.ee/et/Item/58b0b89d-b1ba-4a73-ba53-850910d697b5> https://www.ester.ee/record=b5491885*est

Mikk Raud: Eestil on aeg oma kiibipotentsiaal ellu äratada

Arjakas, Merili diplomaatia.ee 2023

Mikroelektroonika kiipide testimise tarkvara turbo-tester : kommentaar Eesti Teaduste Akadeemia Bernhard Schmidt'i preemia pälvinud tööle

Raik, Jaan Tallinna Tehnikaülikooli aastaraamat 2007 2008 / lk. 275-278

Miks on oskus kiipe luua Eesti jaoks oluline?

Raik, Jaan; Ubar, Raimund-Johannes postimees.ee 2025 <https://arvamus.postimees.ee/8313767/jaan-raik-raimund-ubar-miks-on-oskus-kiipe-luua-estti-jaoks-oluline>

Mitut kiipsüsteemi on vaja?

Tammemäe, Kalle A & A 2002 / 6, lk. 51-54

Model synthesis from VHDL for the functional test generation system

Krupnova, Helena 1993 https://www.ester.ee/record=b2090509*est

NOC mapping and scheduling

Nikiforov, Deniss Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 73-78 : ill

Novel data dependent divider circuit block implementation for complex division and area critical applications

Patankar, Udayan Sunil; Flores, Miguel E.; Koel, Ants Scientific reports 2023 / art. 3027, 28 p. : ill <https://doi.org/10.1038/s41598-023-28343-3> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Nädala lood: jätkuvad halvad uudised ehitusest

Rõuk, Viivika aripaev.ee 2023 [Nädala lood: jätkuvad halvad uudised ehitusest](#)

Nööpmälu iButton

Toomsalu, Arvo A & A 2007 / 5, lk. 8-17 : ill https://artiklid.elnet.ee/record=b1021105*est

Off-line testing of crosstalk induced glitch faults in NoC Interconnects

Bengtsson, Tomas; Kumar, Shashi; Jutman, Artur; Ubar, Raimund-Johannes Proceedings [of] 24th IEEE Norchip Conference : Linköping, Sweden, 20-21 November 2006 2006 / p. 221-225 : ill <http://dx.doi.org/10.1109/NORCHIP.2006.329215>

Off-line testing of delay faults in NoC interconnects

Bengtsson, Tomas; Jutman, Artur; Kumar, Shashi; Peng, Zebo; Ubar, Raimund-Johannes 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 677-680 : ill <http://dx.doi.org/10.1109/DSD.2006.72>

On the combined use of HLDDs and EFSMs for functional ATPG

Di Guglielmo, Giuseppe; Fummi, Franco; Jenihhin, Maksim; Pravadelli, Graziano; Raik, Jaan; Ubar, Raimund-Johannes 5th IEEE East-West Design & Test Symposium EWDTS 2007 : September 7-10, 2007, Yerevan, Armenia 2007 / p. 503-508 : ill

Optimization of the store-and-generate based built-in self-test

Ubar, Raimund-Johannes; Jervan, Gert; Kruus, Helena; Orasson, Elmet; Aleksejev, Igor BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 199-202 : ill

OTA-C realization of PIA brake and throttle controllers for autonomous vehicles

Dimeas, Ilias; Psychalinos, Costas; Elwakil, Ahmed; **Tepljakov, Aleksei** 2017 European Conference on Circuit Theory and Design (ECCTD 2017) : Catania, Italy, 4 - 6 September, 2017 / p. 39-40 : ill <http://dx.doi.org/10.1109/ECCTD.2017.8093229>

Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems

Ubar, Raimund-Johannes Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 303-324 : ill <http://dx.doi.org/10.2298/FUEE1103303U>

Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems

Ubar, Raimund-Johannes Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 1-10 : ill <https://scindeks-clanci.ceon.rs/data/pdf/0353-3670/2011/0353-36701103303U.pdf>

Overview of recent steady state analysis methods

Jokinen, Hannu; Valtonen, Martti BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 277-280: ill

Pooljuhtkomponentide simuleerimine arvutil : laboratoorse töö juhend

2003 http://www.ester.ee/record=b1766958*est

A pragmatic methodology for blind hardware trojan insertion in finalized layouts

Hepp, Alexander; **Perez, Tiago Diadami; Pagliarini, Samuel Nascimento**; Sigl, Georg ICCAD '22: Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design 2022 / art. 69, p. 1-9 : ill <https://doi.org/10.1145/3508352.3549452>
[Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Preface

Hollstein, Thomas; Raik, Jaan; Kostin, Sergei; Tšertov, Anton; O'Connor, Ian; Reis, Ricardo VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability, 24th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2016, Tallinn, Estonia, September 26-28, 2016 : Revised Selected Papers 2017 / p. V-VI
<https://link.springer.com/book/10.1007/978-3-319-67104-8> [Conference proceedings at Scopus](#) [Article at Scopus](#)

Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia

2012 http://www.ester.ee/record=b2777270*est

Propellerkiip

Tammemäe, Kalle A & A 2006 / 5, lk. 6-14 : ill

Rahvusvaheline süsteem-kiibil teaduskonverents Soomes - Tampere SoC Symposium 2003

Raik, Jaan A & A 2003 / 6, lk. 56

Real-time regulation of beam-based feedback : implementing an FPGA solution for a continuous wave linear accelerator

Maalberg, Andrei; Kuntzsch, Michael; **Petlenkov, Eduard** Sensors 2022 / art. 6236, 22 p. : ill <https://doi.org/10.3390/s22166236>
[Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

RESAA: A Removal and Structural Analysis Attack Against Compound Logic Locking

Almeida, Felipe; Aksoy, Levent; Pagliarini, Samuel Nascimento IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2025 / p. 1348-1360 <https://doi.org/10.1109/TVLSI.2025.3534658>

RESAA: A Removal and Structural Analysis Attack Against Compound Logic Locking : [preprint]

Almeida, Felipe; Aksoy, Levent; Pagliarini, Samuel Nascimento arXiv.org 2025 / 12 p. : ill <https://doi.org/10.48550/arXiv.2409.16959>

Reseeding using compaction of pre-generated LFSR sequences

Jutman, Artur; Aleksejev, Igor; Raik, Jaan; Ubar, Raimund-Johannes ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : 31st August to 3rd September 2008, Malta : conference guide 2008 / p. 215

Reseeding using compaction of pre-generated LFSR sub-sequences

Jutman, Artur; Aleksejev, Igor; Raik, Jaan; Ubar, Raimund-Johannes ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : Malta 2008 / p. 1290-1295 : ill <http://dx.doi.org/10.1109/ICECS.2008.4675096>

Re-using chip level DFT at board level

Gu, Xinli; **Jutman, Artur** Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th–June 1st, 2012, Annecy, France 2012 / 1 p https://www.academia.edu/25351525/Re_using_chip_level_DFT_at_board_level

Reusing verification assertions as security checkers for Hardware Trojan detection

Eslami, Mohammad; Ghasempouri, Tara; Pagliarini, Samuel Nascimento 2022 23rd International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA : 06-07 April 2022 2022 / p. 1-6 : ill <https://doi.org/10.1109/ISQED54688.2022.9806292>

SCARF : securing chips with a robust framework against fabrication-time hardware trojans

Eslami, Mohammad; Ghasempouri, Tara; Pagliarini, Samuel Nascimento IEEE Transactions on Computers 2024 / p. 2761-2775 <https://doi.org/10.1109/TC.2024.3449082> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Second IEEE East-West Design and Test Workshop

Hahanov, Vladimir; Ubar, Raimund-Johannes IEEE journal of design & test of computers 2004 / p. 594

Security-aware physical synthesis of integrated circuits = Integraallülituste turvateadlik füüsiline süntees

Perez, Tiago Diadami 2023 <https://doi.org/10.23658/taltech.4/2023> <https://digikogu.taltech.ee/et/Item/440f41fd-0950-4b5c-8e47-4f75a754cdae> https://www.ester.ee/record=b5536743*est

Sensortehnoloogia põhised kiibid on Eesti võimalus : Alar Kuusik: „Ootan väga, et ühiskonnas tuleks tagasi vastuvõtlikkus uutele, ka radikaalsetele lahendustele ja reformidele.“

Kuusik, Alar sirp.ee 2025 <https://www.sirp.ee/sensortehnoloogia-pohised-kiibid-on-estti-voimalus/>

Shift register based TPG for at-speed interconnect BIST

Jutman, Artur MIEL 2004 : 24th International Conference on Microelectronics : Niš, Serbia and Montenegro, 16-19 May 2004 : proceedings. Volume 2 2004 / p. 751-754 : ill <https://ieeexplore.ieee.org/document/1314941?signout=success>

Side-channel attacks on triple modular redundancy schemes

Almeida, Felipe; Aksoy, Levent; Raik, Jaan; Pagliarini, Samuel Nascimento 2021 IEEE 30th Asian Test Symposium ATS 2021 : proceedings 2021 / p. 79-84 : ill <https://doi.org/10.1109/ATS52891.2021.00026> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

A side-channel hardware trojan in 65nm CMOS with 2μW precision and multi-bit leakage capability

Perez, Tiago Diadami; Pagliarini, Samuel Nascimento 2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC) : 17-20 January 2022 : Taipei, Taiwan 2022 / p. 9-10 : ill <https://doi.org/10.1109/ASP-DAC52403.2022.9712490>

Side-channel Trojan insertion - a practical foundry-side attack via ECO

Perez, Tiago Diadami; Imran, Malik; Vaz, Pablo; Pagliarini, Samuel Nascimento 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, May 22-28, 2021 : proceedings 2021 / 5 p. : ill <https://doi.org/10.1109/ISCAS51556.2021.9401481> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Silicon integrated circuit fabrication process modeling and simulation

Rang, Toomas; Tamay, K.; Mizsei, Janos Periodica polytechnica. Electrical engineering = Электротехника 1980 / p. 109-113 https://www.ester.ee/record=b1198855*est

A simulation framework for 3-dimension networks-on-chip with different vertical channel density configurations

Ying, Haoyuan; Jaiswal, Ashok; Abd El Ghany, Mohamed A; Hollstein, Thomas; Hofmann, Klaus Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia 2012 / p. 83-88 : ill

Split-chip design to prevent IP reverse engineering

Pagliarini, Samuel Nascimento; Sweeney, Joseph; Mai, Ken; Blanton, Shawn; Mitra, Subhasish; Pileggi, Larry IEEE Design and Test 2020 / p. 109-118 <https://doi.org/10.1109/MDAT.2020.3033255> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

State assignment for CMOS implementation of low power FSM networks

Zaugarov, Viktor; Kasirova, Lilia; Tveretina, Olga Mixed Design of Integrated Circuits and Systems : education of computer aided design of modern ICs and devices : 3rd Advanced Training Course, Lodz, Poland, 30 May - 1 June 1996 1996 / p. 195-198: ill

Steady state analysis of an output signal based combination of two NLMS adaptive filters

Trump, Tõnu 17th European Signal Processing Conference (EUSIPCO 2009) : 24-28 August 2009 2009 / p. 1720-1724 <https://ieeexplore.ieee.org/document/7077570>

Steady state analysis of the galvanically isolated DC/DC converter with a commutating LC filter [Electronic resource]

Zakis, Janis; Vinnikov, Dmitri; Rankis, Ivars 2012 IEEE International Conference on Industrial Technology : proceedings CD 2012 / p. 838-843 : ill [CD-ROM] <https://ieeexplore.ieee.org/document/6210041>

Structurally synthesized multiple input BDDs for simulation of digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunisia, 13-19 December, 2009 2009 / p. 451-454 : ill <http://dx.doi.org/10.1109/ICECS.2009.5410895>

A survey on split manufacturing : attacks, defenses, and challenges

Perez, Tiago Diadami; Pagliarini, Samuel Nascimento IEEE Access 2020 / p. 184013-184035

<https://doi.org/10.1109/ACCESS.2020.3029339> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Süvatehnoloogiate alternatiivsed arengutrajektoorid ja nende tähendus Eestile : lõpparuanne

Koppel, Kaupo; Kuusik, Alar; Arrak, Kadri; **Raik, Jaan; Niidu, Allan**; Kõks, Kerttu-Liis; **Lahtvee, Petri-Jaan** 2023

<https://media.voog.com/0000/0037/5345/files>

Symmetry in the narrow sense: on the linearity and time-invariance of DQ0 models

Segev, Elior; Ofir, Ron; **Belikov, Juri**; Levron, Yoash IEEE Transactions on Power Systems 2023 / p. 1751-1754

<https://doi.org/10.1109/TPWRS.2022.3229873> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Synthesis of multiple fault oriented test groups from single fault test sets [Electronic resource]

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan 2013 8th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS) : 26-28 March 2013, Abu Dhabi, UAE 2013 / p. 36-41 : ill [CD-ROM]

Synthesis of sequential circuits with dynamic power management

Lensen, Harri; Kruus, Margus; Sudnitsõn, Aleksander Proc. of 42nd International Scientific Conference of Riga Technical University : RTUCET'01 2001 / p. 81-86

Synthesis of sequential circuits with dynamic power management

Lensen, Harri; Kruus, Margus; Sudnitsõn, Aleksander Scientific proceedings of Riga Technical University. 7.serija, Telecommunications and electronics 2001 / p. 81-86

A system for teaching basic and advanced topics of IEEE 1149.1 boundary scan standard (extended abstract)

Jutman, Artur; Rosin, Vjatšeslav; **Sudnitsõn, Aleksander; Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich Proceedings of 16th EAEEIE Conference on Innovation in Education for Electrical and Information Engineering (EIE) : Lappeenranta, Finland, 6th-8th June 2005 2005 / [2] p. : ill

System level power-performance trade-offs in embedded systems using voltage and frequency scaling of off-chip buses and memory

Puttaswamy, Kiran; Choi, Kyu-Won; Park, Jun Cheol; Mooney III, Vincent J.; Chatterjee, Abhijit; **Ellervee, Peeter** ISSS'02, October 2-4, 2002, Kyoto, Japan 2002 / p. 225-230 : ill <https://ieeexplore.ieee.org/document/1227182>

System-level data format exploration for dynamically allocated data structures

Ellervee, Peeter; Miranda, Miguel; Catthoor, Francky; Hemani, Ahmed IEEE transactions on computer-aided design of integrated circuits and systems 2001 / 12, p. 1469-1472 : ill <https://ieeexplore.ieee.org/abstract/document/969440>

System-level design of timing-sensitive network-on-chip based dependable systems = Kiipvõrkudel põhinevate ajakriitiliste ja töökindlate süsteemide kõrgtaseme disain

Tagel, Mihkel 2012 https://www.ester.ee/record=b2778263*est

Z-RAM-mälu

Toomsalu, Arvo A & A 2008 / 3, lk. 10-19 https://artiklid.elnet.ee/record=b1022321*est

TalTech panustab kosmosevaldkonda kiipide, päikesepaneelide ja satelliitidega

Normak, Liisu Kirke Trialoog 2025 <https://trialoog.taltech.ee/taltech-panustab-kosmosevaldkonda-kiipide-paikesepaneelide-ja-satelliitidega/>

TalTech professor: AI chip restrictions on Estonia won't make much difference

Tammet, Tanel news.err.ee 2025 [TalTech professor: AI chip restrictions on Estonia won't make much difference](#)

TalTechi arvutisüsteemide professori uudne tehnoloogia raskendab spionaaži [Võrguväljaanne]

Kald, Indrek ituudised.ee 2021 ["TalTechi arvutisüsteemide professori uudne tehnoloogia raskendab spionaaži"](#)

Tammet: USA kiibipiirang Eestit ei mõjuta

Tammet, Tanel err.ee 2025 [Tammet: USA kiibipiirang Eestit ei mõjuta](#)

Targeting conditional operations in sequential test pattern generation

Raik, Jaan; Ubar, Raimund-Johannes 9th European Test Symposium : ETS'04 : Congress Center, Ajaccio, Corsica, France, May 23-26, 2004 2004 / p. 17-18 : ill

https://www.researchgate.net/publication/239717327_Targeting_Conditional_Operations_in_Sequential_Test_Pattern_Generation

Teaching advanced test issues in digital electronics

Ubar, Raimund-Johannes; Orasson, Elmet; Raik, Jaan; Wuttke, Heinz-Dietrich Proceedings of the 6th IEEE International Conference on Information Technology Based Higher Education and Training : ITHET : July 7-9, 2005, Juan Dolio, Dominican Republic 2005 / p. S2B-1 - S2B-6 : ill <http://dx.doi.org/10.1109/ITHET.2005.1560318>

Teaching digital test with BIST analyzer

Jutman, Artur; Tšertov, Anton; Tšepurov, Anton; Aleksejev, Igor; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 19th EAAEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 123-128 : ill <http://dx.doi.org/10.1109/EAAEIE.2008.4610171>

Tehisintellekti kiire areng töötab kiibitööstust põhjalikult raputada

Port, Kristjan delfi.ee 2023 [Tehisintellekti kiire areng töötab kiibitööstust põhjalikult raputada](#)

Tehnikaülikooli teadlased loovad uue põlvkonna veakindlaid kiipe

Nõges, Krõõt Mente et Manu 2010 / lk. 2 https://www.ester.ee/record=b1242496*est

Tehnikaülikooli teadlaste juhtimisel luuakse uue põlvkonna veakindlaid kiipe

Studiosus 2010 / veebr., lk. 8 https://www.ester.ee/record=b1558644*est

10th IEEE European Test Symposium

Ubar, Raimund-Johannes; Prinetto, Paolo; **Raik, Jaan** IEEE journal of design & test of computers 2005 / p. 480-481 : phot <http://dx.doi.org/10.1109/MDT.2005.106>

Test configurations for diagnosing faulty links in NoC switches

Raik, Jaan; Ubar, Raimund-Johannes; Govind, Vineeth 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 29-34 : ill <http://dx.doi.org/10.1109/ETS.2007.41>

Test cost minimization for hybrid BIST

Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes** IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems : 25-27 October 2000, Yamanashi, Japan : proceedings 2000 / p. 283-298 : ill <https://ieeexplore.ieee.org/abstract/document/887168>

Test methods for crosstalk-induced delay and glitch faults in network-on-chip interconnects implementing asynchronous communication protocols

Bengtsson, Tomas; Kumar, Shashi; **Ubar, Raimund-Johannes; Jutman, Artur;** Peng, Zebo IET computers and digital techniques 2008 / 6, p. 445-460 https://www.diva-portal.org/smash/record.jsf?dswid=-5073&aq2=%5B%5B%5D%5D&c=39&af=%5B%5D&searchType=SIMPLE&sortOrder2=title_sort_asc&language=en&pid=diva2%3A290043&aq=%5B%5B%7B%22personId%22%3A%22authority-person%3A23389%22%7D%5D%5D&sf=all&aq=%5B%5D&sortOrder=author_sort_asc&onlyFullText=false&noOfRows=50

Test time minimization for hybrid BIST of core-based systems

Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes; Jenihhin, Maksim** 12th Asian Test Symposium (ATS 2003) : 17-19 November 2003, Xian, China 2003 / p. 318-325 : ill <https://link.springer.com/article/10.1007/s11390-006-0907-x>

Test time minimization for hybrid BIST with test pattern broadcasting

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Zebo IEEE NORCHIP 2003 : 21 Norchip Conference : Riga, Latvia, 10-11 November 2003 : proceedings 2003 / p. 112-116 : ill <https://www.ida.liu.se/labs/eslab/publications/pap/db/norchip03.pdf>

Testability analysis for efficient register-transfer level test generation [Electronic resource]

Nõmmeots, Tanel; Raik, Jaan; Ubar, Raimund-Johannes 9th International Conference MIXDES 2002 : Mixed Design of Integrated Circuits and Systems, Wroclaw, Poland, 20-22 June 2002 2002 / [4] p. [CD-ROM]

The dildis-project-using applets for more demonstrative lectures in digital systems design and test

Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich FIE 2001 : 31st Annual Frontiers in Educations Conference : Impact on Engineering and Science Education : Reno, Nevada, October 10-13, 2001 : conference program 2001 / p. 83 <https://ieeexplore.ieee.org/document/963996>

The dildis-project-using applets for more demonstrative lectures in digital systems design and test

Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of the 31st ASEE/IEEE Frontiers in Educations Conference : FIE'2001 : Reno, Nevada 2001 / p. SIE-2-7 <https://ieeexplore.ieee.org/document/963996>

Töökindla arvutusriistvara keskuse juht Maksim Jenihhin

Jenihhin, Maksim forte.delfi.ee 2024 [Töökindla arvutusriistvara keskuse juht Maksim Jenihhin](#)

Ultra fast parallel fault analysis on structurally synthesized BDDs

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 131-136 : ill <http://dx.doi.org/10.1109/ETS.2007.43>

Untestable fault identification in sequential circuits using model-checking

Raik, Jaan; Fujiwara, Hideo; Ubar, Raimund-Johannes; Krivenko, Anna Proceedings of the 17th Asian Test Symposium ATS 2008 : November 24-27, 2008, Sapporo, Japan 2008 / p. 21-26 : ill <http://dx.doi.org/10.1109/ATS.2008.22>

Using Tabu search method for optimizing the cost of hybrid BIST

Kruus, Helena; **Ubar, Raimund-Johannes; Jervan, Gert**; Peng, Z. XVI Conference on Design of Circuits and Integrated Systems : Porto, Portugal, 2001 2001 / p. 445-450 <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=e97bb394ff71aa0affcc5fb372404bbc246888a8>

Utilizing layout effects for analog logic locking

Aljafar, Muayad J.; Azais, Florence; Flottes, Marie-Lise; Pagliarini, Samuel Journal of Cryptographic Engineering 2024 / p. 311-324 <https://doi.org/10.1007/s13389-024-00350-8> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Uudne turvaline kiibitehnoloogia

Raik, Jaan Mente et Manu 2021 / lk. 32-33 : fot [Mente et Manu 2/2021](#)

Uuring: Eesti majanduse veduriks võib saada kuus tehnoloogiavaldkonda

Bioneer.ee 2023 [Uuring: Eesti majanduse veduriks võib saada kuus tehnoloogiavaldkonda](#)

Versatile direct and transpose matrix multiplication with chained operations : an optimized architecture using circulant matrices

Iakymchuk, Taras; Rosado-Munoz, Alfredo; Mompean, Manuel Bataller; Villora, Jose Vicente Frances; **Osimiry, Emmanuel Ovie** IEEE Transactions on Computers 2016 / p. 3470 - 3479 <https://doi.org/10.1109/TC.2016.2538235> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

VHDL design debug framework based on zamiaCAD

Tihhomirov, Valentin; Tšepurov, Anton; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill

Võitlus kiipides varitsevate troojalastega tõstab Eesti teadlased kilbile

Härmat, Karin err.ee 2023 [Võitlus kiipides varitsevate troojalastega tõstab Eesti teadlased kilbile](#)

XXI sajandi arvuti

Toomsalu, Arvo A & A 2000 / 1, lk. 8-13 ; 2, lk. 8-19 https://artiklid.elnet.ee/record=b1003324*est

Быстродействующие интегральные компараторы

Gurjanov, Boris; Tamm, Uljas IX Всесоюзная научно-техническая конференция по микроэлектронике, г. Казань, 14-17 окт. 1980 г. : тезисы докладов 1980 / с. 88

Генерирование тестов для микропроцессорных БИС

Viilup, Agu; Evarston, Teet Расчет и проектирование систем технической кибернетики 1983 / с. 121-129 : ил https://www.ester.ee/record=b1288991*est <https://digikogu.taltech.ee/et/Item/7d7515af-76b7-4d35-89a7-e80367d5b635>

Изменение параметров интегральных схем при анализе в растровом электронном микроскопе

Meiler, Boriss Электрофизические свойства полупроводниковых и диэлектрических материалов 1986 / с. 85-92 https://www.ester.ee/record=b1296001*est

Измеритель коэффициента шума интегральных усилителей

Tammet, Heinar; Torim, A.A. Тезисы докладов республиканской научно-технической конференции, посвященной 80-летию со дня изобретения радио А. С. Поповым 1975 / с. 93 https://www.ester.ee/record=b1322122*est

Измеритель шумов интегральных схем

Koiduste, A.; Tammet, Heinar XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с. 147 https://www.ester.ee/record=b1306141*est

Исследование влияния технологического микроклимата в производстве интегральных микросхем : автореферат ... кандидата технических наук (05.12.18)

Rätsep, Ülo 1983 https://www.ester.ee/record=b1522476*est

Коэффициентное ударное ионизации носителей заряда в <100> арсениде галлия

Rang, Toomas; Puusepp, Märt Электронная техника. Серия 2, Полупроводниковые приборы : научно-технический сборник 1987 / с. 98-100 https://www.ester.ee/record=b2160501*est

Математическая модель для задания структуры и функций микропроцессорных БИС

Lohuaru, Tõnu; Räisa, O.; Toome, T. Методы синтеза и диагностирования цифровых схем 1985 / с. 75-81 : ил https://www.ester.ee/record=b1302568*est <https://digikogu.taltech.ee/et/Item/e00f2c15-fd8c-48ac-9963-76da1d62d592>

Метод исследования комплексного влияния параметров технологического микроклимата на качество полупроводниковых интегральных микросхем

Rätsep, Ülo Тезисы докладов Республиканской научно-технической конференции "Современные методы и устройства радиоэлектронного оборудования", посвященной Дню радио. Секция: полупроводниковые приборы 1981 / с. 81-82
https://www.ester.ee/record=b1310801*est

Метод исследования технологического процесса производства интегральных микросхем, основанный на анализе кластеров состояний

Rätsep, Ülo; Teevet, J.-T. Методы и средства обработки сигналов при наличии шумов 1982 / с. 39-43

https://www.ester.ee/record=b1312255*est <https://www.etera.ee/zoom/121735/view?page=1&p=separate&search=true&tool=search>

Методическое пособие к лабораторным работам и курсовому проектированию по дисциплине "Схемотехника ЭВМ"

1987 https://www.ester.ee/record=b1354263*est

Методы идентификации шумовых источников интегральных схем

Tammet, Heinar Тезисы докладов республиканской научно-технической конференции, посвященной Дню радио, Таллин, 1977

1977 / с. 87-88 https://www.ester.ee/record=b1313776*est

Оценка тенденции использования некоторых видов микросхем

Maltsev, Jüri; Ševtšenko, S. Тезисы докладов республиканской научно-технической конференции, посвященной Дню радио. [1], Секция: Информационно-измерительная техника 1981 / с. 25-26 https://www.ester.ee/record=b1310782~S1*est

Построение тестов для неисправностей комбинационных схем на основе анализа ортогональных дизъюнктивных нормальных форм, представляемых альтернативными графами

Matrosova, A.Yu.; Pleshkov, A.G.; Ubar, Raimund-Johannes Автоматика и телемеханика 2005 / с. 158-174 : ил

<http://mi.mathnet.ru/at1333>

Прогнозирование качества интегральных микросхем на основе кластеров состояний

Budarin, Vladimir; Rätsep, Ülo; Teevet, J.-T. Методы и средства цифровой обработки сигналов 1984 / с. 111-115

https://www.ester.ee/record=b1302208*est <https://digikogu.taltech.ee/et/Item/e49ece5a-b726-4a2f-860f-748b84670a0c>

«Сейчас время больших перемен»: профессор TalTech приоткрыл завесу тайны развития ИИ в Эстонии

Grebneva, N.; Jenihhin, Maksim rus.postimees.ee 2025 [«Сейчас время больших перемен»: профессор TalTech приоткрыл завесу тайны развития ИИ в Эстонии](#)

Системное исследование влияния технологического микроклимата на качество интегральных микросхем

Rätsep, Ülo Методы обработки и регистрации сигналов 1981 / с. 53-58 : илл https://www.ester.ee/record=b1507633*est

<https://digikogu.taltech.ee/et/Item/b58bba27-822f-44c3-8387-50d8a26bb3d3>

Таммет: ограничения США на поставки чипов не окажут влияния на Эстонию

Tammet, Tanel rus.err.ee 2025 [Таммет: ограничения США на поставки чипов не окажут влияния на Эстонию](#)

Ученый-компьютерщик: ограничения США на поставки чипов замедлят цифровое развитие Эстонии

rus.err.ee 2025 [Ученый-компьютерщик: ограничения США на поставки чипов замедлят цифровое развитие Эстонии](#)

эффективное средство защиты от дронов-камикадзе еще только предстоит найти [Online resources]

rus.err.ee 2022 [AK.Nädal: эффективное средство защиты от дронов-камикадзе еще только предстоит найти](#)