

Automated design error localization in RTL designs

Jenihhin, Maksim; Tšepurov, Anton; Tihhomirov, Valentin; Raik, Jaan; Hantson, Hanno; Ubar, Raimund-Johannes; Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich IEEE design & test of computers 2014 / p. 83-92 : ill
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Test synthesis with alternative graphs

Ubar, Raimund-Johannes IEEE design & test of computers 1996 / Spring, p. 48-57: ill