

Fast test pattern generation for sequential circuits using decision diagram representations

Raik, Jaan; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications (JETTA) 2000 / 3, p. 213-226 : ill
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Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits

Jenihhin, Maksim; Squillero, Giovanni; Tihomirov, Valentin; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill <https://doi.org/10.1007/s10836-016-5589-x> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Identifying untestable faults in sequential circuits using test path constraints

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Optimization of boundary scan tests using FPGA-based efficient scan architectures

Aleksejev, Igor; Devadze, Sergei; Jutman, Artur; Shubin, Konstantin Journal of electronic testing : theory and applications (JETTA) 2016 / p. 245-255 : ill <https://doi.org/10.1007/s10836-016-5588-y> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)