

### **Defect oriented fault coverage of 100stuck-at fault test sets**

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 7th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2000 : Gdynia, Poland, 15-17 June 2000 2000 / p. 511-516 : ill

### **Defect-oriented library builder and hierarchical test generation**

Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Györ, Hungary, April 18-20, 2001 2001 / p. 163-168 : ill

### **Defect-oriented test generation using probabilistic estimation**

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### **Hierarchical defect level test quality analysis**

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** VILAB User Forum 2000 / [11] p

### **Hierarchical defect-oriented fault simulation for digital circuits**

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### **Hierarchical defect-oriented fault simulation for digital circuits**

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### **Hierarchical test generation for combinational circuits with real defects coverage**

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### **Internet-based collaborative test generation with MOSCITO [Electronic resource]**

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### **Test pattern generation at the behavioral level from VHDL circuit description containing several processes**

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