

A new testability calculation method to guide RTL test generation

Raik, Jaan; Nõmmeots, Tanel; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2005 / p. 71-82 : ill <https://doi.org/10.1007/s10836-005-5288-5>

Design error diagnosis with re-synthesis in combinational circuits

Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2003 / 1, p. 73-82 : ill <https://link.springer.com/article/10.1023/A:1021948013402>

High-Level Implementation-Independent Functional Software-Based Self-Test for RISC Processors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Journal of electronic testing : theory and applications 2020 / p. 87-103 <https://doi.org/10.1007/s10836-020-05856-7>

On the reuse of TLM mutation analysis at RTL

Guarnieri, Valerio; **Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2012 / p. 435-448 : ill <https://link.springer.com/article/10.1007/s10836-012-5303-6>

PSL assertion checking using temporally extended high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2009 / 6, p. 289-300 : ill https://pld.ttu.ee/home/maksim/phd_papers/%5B11%5D%20latw%2708.pdf