

An approach for verification assertions reuse in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Fujiwara, Hideo; Ubar, Raimund-Johannes; Viilukas, Taavi Digest of papers : IEEE 11th Workshop on RTL and High Level Testing : WRTL'T'10 : December 5-6, 2010, Shanghai, China 2010 / p. 107-110 : ill

An approach for verification assertions reuse 2 in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Fujiwara, Hideo Journal of Shanghai Normal University : Natural Sciences 2010 / p. 441-447 : ill

https://www.researchgate.net/publication/240613999_An_Approach_for_Verification_Assertions_Reuse_in_RTL_Test_Pattern_Generation

Approaches to improve hierarchical ATPG for synchronous sequential circuits

Viilukas, Taavi Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kuuenda aastakonverentsi artiklite kogumik : 3.-5. oktoobril 2012, Laulasmaa 2012 / p. 105-108 : ill

Automated test bench generation for high-level synthesis flow ABELITE

Viilukas, Taavi; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Baranov, Samary Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2011) : Sevastopol, Ukraine, September 9-12, 2011 2011 / p. 13-16 : ill

<https://ieeexplore.ieee.org/document/6116601>

Automated test pattern generator with constraint solver

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 33-36

Automatic generation of EFSMs and HLDDs for functional ATPG

Tšepurov, Anton; Guglielmo, Giuseppe di; Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 143-146 : ill

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Raik, Jaan; Rannaste, Anna; Jenihhin, Maksim; Viilukas, Taavi; Ubar, Raimund-Johannes; Fujiwara, Hideo Sixteenth IEEE European Test Symposium : 23-27 May 2011, Trondheim 2011 / p. 147-152

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Viilukas, Taavi; Raik, Jaan; Ubar, Raimund-Johannes; Rannaste, Anna; Jenihhin, Maksim; Fujiwara, Hideo Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 139-142 : ill

Constraint-based test pattern generation at the register-transfer level

Viilukas, Taavi; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Krivenko, Anna Proceedings of the 13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 14-16, 2010, Vienna, Austria 2010 / p. 352-357 : ill
<http://dx.doi.org/10.1109/DDECS.2010.5491752>

Constraints solving based hierarchical test generation for synchronous sequential circuits = Kitsenduste lahendamisel baseeruv hierarhiline testigeneerimine sünkroonsetele järjestikiskeemidele

Viilukas, Taavi 2012 https://www.ester.ee/record=b2888278*est

Generating directed tests for C programs using RTL ATPG

Raik, Jaan; Drenkhan, Tiia; Jenihhin, Maksim; Viilukas, Taavi; Karputkin, Anton; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the IEEE 13th Workshop on RTL and High Level Testing (WRTL'T'12) 2012 / p. 1-6

High-level decision diagram based fault models for targeting FSMs

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 353-358 : ill <http://dx.doi.org/10.1109/DSD.2006.60>

Identifying untestable faults in sequential circuits using test path constraints

Viilukas, Taavi; Karputkin, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill <https://link.springer.com/article/10.1007/s10836-012-5312-5>

Mixed hierarchical-functional fault models for targeting sequential cores

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Jenihhin, Maksim Journal of systems architecture 2008 / 3/4, p. 465-477 : ill <https://www.sciencedirect.com/science/article/abs/pii/S1383762107001166>

Using constraint solver in Test Pattern Generation Tool

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 14-17 : ill

Using test pattern generation tool decider in hardware verification

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 166-169 : ill