A scalable model based RTL framework zamiaCAD for static analysis
Tšepurov, Anton; **Jenihhin, Maksim**; **Raik, Jaan**; **Tihhomirov, Valentin** 2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC) : October 7-10, 2012 Santa Cruz, USA Dream Inn, Santa Cruz, USA : [proceedings] 2012 / p. 171-176 : ill https://www.semanticscholar.org/paper/A-scalable-model-based-RTL-framework-zamiaCAD-for-Tsepurov-Bartsch/d19eefa44f793621d537c06498784e06e0332fd2

Application of high-level decision diagrams for simulation-based verification tasks
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Estonian journal of engineering 2010 / 1, p. 56-77 : ill

Applications of the open source HW design framework zamiaCAD
Tšepurov, Anton; **Tihhomirov, Valentin**; **Saif Abrar, Syed**; **Jenihhin, Maksim**; **Raik, Jaan** DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p

APRICOT : a framework for teaching digital systems verification
Raik, Jaan; **Jenihhin, Maksim**; **Tšepurov, Anton**; **Reinsalu, Uljana**; **Ubar, Raimund-Johannes** 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 172-177 : ill http://dx.doi.org/10.1109/EAEEIE.2008.4610181

Assertion checking with PSL and high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Digest of papers IEEE 8th Workshop on RTL and High Level Testing : WRTLT'07 : October 12-13, 2007, Beijing, China 2007 / p. 105-110 : ill https://pld.ttu.ee/~maksim/phd_papers/%5B12%5D%20wrtlt%2707.pdf

Assessment of diagnostic test for automated bug localization
Tihhomirov, Valentin; **Tšepurov, Anton**; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [6] p. : ill

Automated design error debug using high-level decision diagrams and mutation operators
Raik, Jaan; **Repinski, Urmas**; **Tšepurov, Anton**; **Hantson, Hanno**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** Microprocessors and microsystems 2013 / p. 505-513 : ill https://doi.org/10.1016/j.micpro.2012.11.004 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Automated design error localization in RTL designs
Jenihhin, Maksim; **Tšepurov, Anton**; **Tihhomirov, Valentin**; **Raik, Jaan**; **Hantson, Hanno**; **Ubar, Raimund-Johannes**; Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich IEEE design & test of computers 2014 / p. 83-92 : ill https://doi.org/10.1109/MDAT.2013.2271420 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Automatic generation of EFSMs and HLDDs for functional ATPG
Tšepurov, Anton; Guglielmo, Giuseppe di; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Viilukas, Taavi** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 143-146 : ill

BIST analyzer : a training platform for SoC testing [Electronic resource]
Jutman, Artur; **Tšertov, Anton**; **Tšepurov, Anton**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich 37th Annual Frontiers in Education Conference : Global Engineering : Knowledge Without Borders, Opportunities Without Passports : Milwaukee, Wisconsin, October 10-13, 2007 2007 / p. S3H-8-S3H-13 : ill. [CD-ROM] http://dx.doi.org/10.1109/FIE.2007.4418125

Code coverage analysis for concurrent programming languages using high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Reinsalu, Uljana**; **Ubar, Raimund-Johannes** Proceedings of the 12th European Workshop on Dependable Computing : EWDC 2009 : Toulouse, France, May 14-15, 2009 2009 / [4] p. : ill https://hal.archives-ouvertes.fr/hal-00381559

Design error diagnosis using backtrace algorithm on decision diagrams
Repinski, Urmas; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Tšepurov, Anton** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

E-learning environment for WEB-based study of testing
Ubar, Raimund-Johannes; **Jutman, Artur**; **Raik, Jaan**; **Devadze, Sergei**; **Jenihhin, Maksim**; **Aleksejev, Igor**; **Tšepurov, Anton**; **Tšertov, Anton**; **Kostin, Sergei**; **Orasson, Elmet**; Wuttke, Heinz-Dietrich Proceedings of the 8th European Workshop on Microelectronics Education : EWME 2010 : Darmstadt, Germany, 10-12 May 2010 2010 / p. 47-52 : ill

Generating directed tests for C programs using RTL ATPG
Raik, Jaan; Drenkhan, Tiia; **Jenihhin, Maksim**; **Viilukas, Taavi**; **Karputkin, Anton**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Proceedings of the IEEE 13th Workshop on RTL and High Level Testing (WRTLT'12) 2012 / p. 1-6

Hardware modeling for design verification and debug = Riistvara modelleerimine disaini verifitseerimise ja silumise jaoks
Tšepurov, Anton 2013 https://www.ester.ee/record=b2963501*est

High-Level Decision Diagram manipulations for code coverage analysis
Minakova, Karina; **Reinsalu, Uljana**; **Tšepurov, Anton**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes**; **Ellervee, Peeter** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level decision diagrams based coverage metrics for verification and test
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Reinsalu, Uljana**; **Ubar, Raimund-Johannes** LATW 2009 : 10th IEEE Latin American Test Workshop : Buzios, Rio de Janero, Brazil, March 2-5, 2009 2009 / [6] p. : ill http://dx.doi.org/10.1109/LATW.2009.4813792

High-level design error diagnosis using backtrace on decision diagrams
Raik, Jaan; **Repinski, Urmas**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Tšepurov, Anton** 28th Norchip Conference : Tampere, Finland, 15-16 November 2010 : conference program and papers 2010 / [4] p. : ill
http://dx.doi.org/10.1109/NORCHIP.2010.5669486

Localization of bugs in processor designs using zamiaCAD framework
Tšepurov, Anton; **Tihhomirov, Valentin**; **Jenihhin, Maksim**; **Raik, Jaan** 13th International Workshop on Microprocessor Test and Verification (MTV 2012) Common Challenges and Solutions : Austin, USA, December 10–12, 2012 2012 / p. 1-6
https://ieeexplore.ieee.org/document/6519733

Mutation analysis with high-level decision diagrams
Hantson, Hanno; **Raik, Jaan**; **Jenihhin, Maksim**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes**; Guglielmo, Giuseppe di; Fummi, Franco LATW2010 : 11th Latin-American TestWorkshop, March 28-31, 2010, Punta del Este, Uruguay 2010 / [6] p. [CD-ROM] https://ieeexplore.ieee.org/document/5550336

On reusability of verification assertions for testing
Jenihhin, Maksim; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Tšepurov, Anton** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 151-154 : ill

PSL assertion checking using temporally extended high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2009 / 6, p. 289-300 : ill https://pld.ttu.ee/home/maksim/phd_papers/%5B11%5D%20latw%2708.pdf

PSL assertion checking with temporally extended high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 49-54 : ill
https://pld.ttu.ee/~maksim/phd_papers/%5B11%5D%20latw%2708.pdf

Simulation-based verification with APRICOT framework using high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 13-16 : ill

zamiaCAD : open source platform for advanced hardware design
Tšepurov, Anton; **Jenihhin, Maksim**; **Raik, Jaan** DATE 2011 University Booth : Design Automation and Test in Europe : Grenoble, France, March 14-18, 2011 2011 / [2] p.: ill

Teaching digital test with BIST analyzer
Jutman, Artur; **Tšertov, Anton**; **Tšepurov, Anton**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 123-128 : ill
http://dx.doi.org/10.1109/EAEEIE.2008.4610171

Temporally extended high-level decision diagrams for PSL assertions simulation
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Proceedings : Thirteenth IEEE European Test Symposium : ETS 2008 : 25-29 May 2008, Verbania, Italy 2008 / p. 61-68 : ill https://ieeexplore.ieee.org/document/4556029

VHDL design debug framework based on zamiaCAD
Tihhomirov, Valentin; **Tšepurov, Anton**; **Saif Abrar, Syed**; **Jenihhin, Maksim**; **Raik, Jaan** DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill