

A new approach to build a low-level malicious fault list starting from high-level description and alternative graphs

Benso, A.; Prinetto, Paolo; Rebaudengo, M.; Sonza, M.; **Ubar, Raimund-Johannes** Proceedings IEEE European Design & Test Conference, Paris, March 17-20, 1997 1997 / p. 560-565 <https://ieeexplore.ieee.org/document/582417>

Exploiting high-level descriptions for circuits fault tolerance assessments

Benso, A.; Prinetto, Paolo; Rebaudengo, M.; Sonza Reorda, Matteo; **Raik, Jaan**; **Ubar, Raimund-Johannes** 1997 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Paris, October 20-22, 1997 1997 / p. 212-216 <https://ieeexplore.ieee.org/document/628327>