

Diagnostic modeling of digital systems with multi-level decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill

High-level decision diagram simulation for diagnosis and soft-error analysis

Raik, Jaan; Repinski, Urmas; Jenihhin, Maksim; Chepurov, Anton Design and test technology for dependable systems-on-chip 2011 / p. 294-309 : ill

High-speed logic level fault simulation

Ubar, Raimund-Johannes; Devadze, Sergei Design and test technology for dependable systems-on-chip 2011 / p. 310-335 : ill

Preface

Ubar, Raimund-Johannes; Raik, Jaan; Vierhaus, Heinrich Theodor Design and test technology for dependable systems-on-chip 2011 / p. xxii-xxviii

Sequential test set compaction in LFSR reseeding

Jutman, Artur; Aleksejev, Igor; Raik, Jaan Design and test technology for dependable systems-on-chip 2011 / p. 476-493 : ill

System-level design of NoC-based dependable embedded systems

Tagel, Mihkel; Ellerjee, Peeter; Jervan, Gert Design and test technology for dependable systems-on-chip 2011 / p. 1-36 : ill