A scalable model based RTL framework zamiaCAD for static analysis
Tšepurov, Anton; **Jenihhin, Maksim**; **Raik, Jaan**; **Tihhomirov, Valentin** 2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC) : October 7-10, 2012 Santa Cruz, USA Dream Inn, Santa Cruz, USA : [proceedings] 2012 / p. 171-176 : ill

Accelerating transient fault injection campaigns by using Dynamic HDL Slicing
Bagbaba, Ahmet Cagri; **Jenihhin, Maksim**; **Raik, Jaan**; Sauer, Christian 2019 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC), 29-30 October 2019, Helsinki, Finland : proceedings in IEEE Xplore 2019 / 7 p. : ill https://doi.org/10.1109/NORCHIP.2019.8906932

Efficient fault injection based on dynamic HDL slicing technique
Bagbaba, Ahmet Cagri; **Jenihhin, Maksim**; **Raik, Jaan**; Sauer, Christian 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 52-53 : ill
https://doi.org/10.1109/IOLTS.2019.8854419

Extensible open-source framework for translating RTL VHDL IP cores to SystemC
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

Mutation analysis for systemC designs at TLM
Guarnieri, Valerio; Bombieri, Nicola; Pravadelli, Graziano; Fummi, Franco; **Hantson, Hanno**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes** 12th IEEE Latin American Test Workshop (LATW) : Porto de Galinhas, Brasil, 27-30 March 2011 2011 / [6] p

Simulation-based equivalence checking between IEEE 1687 ICL and RTL
Damljanovic, Aleksa; **Jutman, Artur**; Portolan, Michele; Tšertov, Anton 2019 IEEE International Test Conference (ITC) 2019 / paper. 7.3, 8 p. : ill https://doi.org/10.1109/ITC44170.2019.9000181