

A synthesis-agnostic behavioral fault model for high gate-level fault coverage

Karputkin, Anton; Raik, Jaan Proceedings of the 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE) : 14-18 March 2016, ICC, Dresden, Germany 2016 / p. 1124-1127 : ill <https://ieeexplore.ieee.org/document/7459477/figures#figures>

Applications of the open source HW design framework zamiaCAD

Tšepurov, Anton; Tihomirov, Valentin; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p

A DFT scheme to improve coverage of hard-to-detect faults in FinFET SRAMs

Cardoso Medeiros, Guilherme; **Gürsoy, Cemil Cem**; Fieback, Moritz; Wu, Lizhou; **Jenihhin, Maksim**; Taouil, Mottaqiallah; Hamdioui, Said 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE), 9-13 March 2020, Grenoble, France : proceedings 2020 / p. 792-797 <https://doi.org/10.23919/DATe48585.2020.9116278>

Fast and optimized task allocation method for low vertical link density 3-Dimensional Networks-on-Chip based many core systems

Ying, Haoyuan; **Hollstein, Thomas**; Hofmann, Klaus Proceedings : Design, Automation & Test in Europe : Grenoble, France, March 18-22, 2013 2013 / p. 1777-1782 : ill

IEEE P1687 IJTAG demonstrator on FPGA

Shibin, Konstantin; Aleksejev, Igor; Jutman, Artur; Devadze, Sergei DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p. : ill

A rescue demonstrator for interdependent aspects of reliability, security and quality towards a complete EDA flow

Raik, Jaan; Jenihhin, Maksim Proceedings of the 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE 2020), 9 to 13 March, 2020, Grenoble, France 2020 / p. 58 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=9116424>

RESCUE: interdependent challenges of reliability, security and quality in nanoelectronic systems

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