An external diagnosis method for network-on-a-chip
Raik, Jaan; Govind, Vineeth; **Ubar, Raimund-Johannes** IEEE/ACM Design Automation and Test in Europe, Workshop on Diagnostic Services in Networks-on-Chips - Test, Debug and On-line Monitoring : April 16-20, 2007, Nice, France 2007 / [2] p. : ill

An external test approach for network-on-a-chip switches
Raik, Jaan; **Govind, Vineeth**; **Ubar, Raimund-Johannes** ATS '06 : Proceedings of the 15th Asian Test Symposium : November 20-23, 2006, Fukuoka, Japan 2006 / p. 437-442 : ill http://dx.doi.org/10.1109/ATS.2006.23

Analysis and comparison of attainable hardware acceleration in all programmable systems-on-chip
Sklyarov, Valery; Skliarova, Iouliia; Silva, João; **Sudnitsõn, Aleksander** Euromicro Conference on Digital System Design : DSD 2015 : 26-28 August 2015, Funchal, Madeira, Portugal : proceedings 2015 / p. 345-352 : ill http://dx.doi.org/10.1109/DSD.2015.45

Architectural exploration tasks for on-chip embedded systems
Reinsalu, Uljana; **Arhipov, Anton**; **Ellervee, Peeter** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 171-174 : ill

Automated minimization of concurrent online checkers for network-on-chips
Saltarelli, Pietro; **Niazmand, Behrad**; **Hariharan, Ranganathan**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 10th International Symposium on Reconfigurable and Communication-centric Systems-on-Chip (ReCoSoC 2015) : Bremen, 29 June - 1 July 2015 2015 / [8] p. : ill http://dx.doi.org/10.1109/ReCoSoC.2015.7238079

AWAIT : an ultra-lightweight soft-error mitigation mechanism for network-on-chip links
Janson, Karl; **Pihlak, Rene**; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Jervan, Gert**; **Raik, Jaan** 2018 13th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), Lille, France, July 9th-11th, 2018 2018 / p. 1-6 : ill https://doi.org/10.1109/ReCoSoC.2018.8449374

Bringing research issues into lab scenarios on the example of SoC testing [Electronic resource]
Ubar, Raimund-Johannes; **Jutman, Artur**; **Devadze, Sergei**; Wuttke, Heinz-Dietrich International Conference on Engineering Education - ICEE 2007 : September 3-7, 2007, Coimbra, Portugal 2007 / [7] p. : ill. [CD-ROM]
http://icee2007.dei.uc.pt/proceedings/papers/429.pdf

CAESAR-MPSoC : dynamic and efficient MPSoC security zones
Azad, Siavoosh Payandeh; Tempelmeier, Michael; **Jervan, Gert**; Sepulveda, Johanna 2019 IEEE Computer Society Annual Symposium on VLSI : ISVLSI 2019 : proceedings 2019 / p. 477-482 : ill https://doi.org/10.1109/ISVLSI.2019.00092

Challenges for future system-on-chip design
Hollstein, Thomas; Peng, Zebo; **Ubar, Raimund-Johannes**; Glesner, Manfred Circuit Paradigm in the 21st Century : ECCTD '01 : proceedings of the 15th European Conference on Circuit Theory and Design : Helsinki University of Technology, Finland, 28th-31st August 2001. Vol 3 2001 / p. 173-176

Code compaction within CGRAs
Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 133-136 : ill

Comprehensive performance and robustness analysis of 2D turn models for network-on-chips
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Janson, Karl**; Kogge, Thilo; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 2017 IEEE International Symposium on Circuits and Systems (ISCAS) 2017 / p. 1476-1479 : ill
https://doi.org/10.1109/ISCAS.2017.8050634

Cost-effective concurrent hardware checkers for network on chip based system on chip = Kulutõhusad süsteemiga paralleelsed rikkemonitorid kiipvõrkudel põhinevatele kiipsüsteemidele
Hariharan, Ranganathan 2019 https://digi.lib.ttu.ee/i/?12854

Cross-layer dependability management in network on chip based system on chip = Kiipvõrkudel põhinevate süsteemide kihtideülene usaldatavuse haldus
Azad, Siavoosh Payandeh 2018 https://digi.lib.ttu.ee/i/?9948

Data-driven cross-layer fault management architecture for sensor networks
Vihman, Lauri; **Kruusmaa, Maarja**; **Raik, Jaan** 16th European Dependable Computing Conference : EDCC 2020 : Virtual Conference, Munich, Germany, 7-10 September 2020 : proceedings 2020 / art. 20094188, p. 33-40
https://doi.org/10.1109/EDCC51268.2020.00015

Deadlock-free generic routing algorithms for 3-dimensional Networks-on-Chip with reduced vertical link density topologies

Ying, Haoyuan; Jaiswal, Ashok; **Hollstein, Thomas**; Hofmann, Klaus Journal of systems architecture 2013 / p. 528-542 : ill

Dependability improvements of NoC-based systems = Töökindluse parandamine kiipvõrkudel põhinevates süsteemides
Niazmand, Behrad 2018 https://digi.lib.ttu.ee/i/?9879

Design and test technology for dependable systems-on-chip
2011 https://www.ester.ee/record=b4467408*est

Design concept and microarchitecture of network-on-chip with best-effort and guaranteed-throughput services
Samman, Faizal; **Hollstein, Thomas** International journal of innovative computing, informationand control 2019 / p. 305–319 : ill https://doi.org/10.24507/ijicic.15.01.305 http://www.ijicic.net/ http://www.ijicic.net/servlet/Download?contentID=CONT5b67c7cbc23142feade914ceeabbdf4d Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Design space exploration and optimisation for NoC-based timing sensitive systems
Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 177-180 : ill

Design space exploration and optimisation for NoC-based timing sensitive systems
Tagel, Mihkel; **Ellervee, Peeter**; **Jervan, Gert** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 117-120 : ill

Design space exploration in multi-level computing systems
Sklyarov, Valery; Skliarova, Iouliia; Silva, João; **Sudnitsõn, Aleksander** CompSysTech'14 : 15th International Conference on Computer Systems and Technologies : Ruse, Bulgaria, June 27-28, 2014 2014 / p. 40-47 : ill

Detecting and mitigating Low-and-Slow DoS attacks in NoC-based MPSoCs
Chaves Arroyave, Cesar Giovanni; **Azad, Siavoosh Payandeh**; Sepulveda, Johanna; **Hollstein, Thomas** 2019 14th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC) : July 1-3 2019, York - United Kingdom : proceedings 2019 / p. 82-89 : ill https://doi.org/10.1109/ReCoSoC48741.2019.9034934

Deterministic traffic generator for network-on-chip simulator
Tagel, Mihkel; **Jervan, Gert** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 72-75 : ill

Deterministic traffic generator for network-on-chip simulator
Tagel, Mihkel; **Jervan, Gert** Workshop Digest. Diagnostic Services in Network-on-Chips - Test, Debug, and On-Line Monitoring : DATE 2007 : Nice, France, 16-20 April, 2007 2007 / p. 288-290

DfT for application of external test patterns in a Network-on-a-Chip
Govind, Vineeth; **Raik, Jaan**; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 25-28 : ill

DfT-based external test and diagnosis of mesh-like networks on chips = Testitavusel põhinev välise testi ja diagnoosi meetod kahemõõtmelistele kiipvõrkudele
Govind, Vineeth 2009 https://digi.lib.ttu.ee/i/?454 https://www.ester.ee/record=b2539211*est

Diagnosing DoS attacks in NoC-based MPSoCs
Chaves Arroyave, Cesar Giovanni; **Azad, Siavoosh Payandeh**; **Hollstein, Thomas**; Sepulveda, Johanna Testmethoden und Zuverlässigkeit von Schaltungen und Systemen, TUZ 2019 2019 / p. [39–41] https://www.researchgate.net/publication/333756736

Diagnostic test generation for statistical bug localization using evolutionary computation
Gaudesi, Marco; **Jenihhin, Maksim**; **Raik, Jaan**; **Tihhomirov, Valentin**; **Ubar, Raimund-Johannes** Applications of Evolutionary Computation : 17th European Conference, EvoApplications 2014, Granada, Spain, April 23-25, 2014 : revised selected papers 2014 / p. 425-436 : ill

A Distributed DoS detection scheme for NoC-based MPSoCs
Chaves Arroyave, Cesar Giovanni; **Azad, Siavoosh Payandeh**; **Hollstein, Thomas**; Sepulveda, Johanna 2018 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC) : 30-31 October 2018, Tallinn, Estonia : proceedings in IEEE Xplore 2018 / 6 p. : ill https://doi.org/10.1109/NORCHIP.2018.8573524

DoS attack detection and path collision localization in NoC-based MPSoC architectures
Chaves Arroyave, Cesar Giovanni; **Azad, Siavoosh Payandeh**; **Hollstein, Thomas**; Sepulveda, Johanna Journal of low power electronics and applications 2019 / art. 7, 20 p. : ill https://doi.org/10.3390/jlpea9010007 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Dynamic and distributed security management for NoC Based MPSoCs
Azad, Siavoosh Payandeh; **Jervan, Gert**; Sepulveda, Johanna Computational Science - ICCS 2019 : 19th International Conference, Faro, Portugal, June 12-14, 2019 : Proceedings, Part II 2019 / p. 649–662 : ill https://doi.org/10.1007/978-3-030-22741-8_4 Conference Proceedings at Scopus Article at Scopud Conference Proceedings at WOS Article at WOS

Dynamic quadrant partitioning adaptive routing algorithm for irregular reduced vertical link density topology 3-dimensional network-on-chips
Ying, Haoyuan; Hofmann, Klaus; **Hollstein, Thomas** Proceedings of the 2014 International Conference on High Performance Computing & Simulation (HPCS 2014) : July 21-25, 2014, Bologna, Italy 2014 / p. 516-522 : ill

Energy-efficient multi-fragment Markov model guided online model-based testing for MPSoC
Vain, Jüri; **Tsiopoulos, Leonidas**; Kharchenko, Vyacheslav; **Apneet Kaur**; **Jenihhin, Maksim**; **Raik, Jaan**; **Nõmm, Sven** Green IT Engineering: Social, Business and Industrial Applications 2019 / p. 273-297 https://doi.org/10.1007/978-3-030-00253-4_12 Article collection at Scopus Article at Scopus

Extended checkers for control part of routers in network-on-chips
Hariharan, Ranganathan; **Niazmand, Behrad**; **Hollstein, Thomas**; **Raik, Jaan**; **Jervan, Gert** MEDIAN 2015 : the 4th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : March 13, 2015, Grenoble, France 2015 / p. 36-39 : ill

Extended checkers for logic-based distributed routing in network-on-chips
Niazmand, Behrad; **Hariharan, Ranganathan**; **Govind, Vineeth**; **Jervan, Gert**; **Hollstein, Thomas**; **Raik, Jaan** BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 77-80 : ill

Extended checkers for logic-based distributed routing in network-on-chips
Niazmand, Behrad; **Hariharan, Ranganathan**; **Govind, Vineeth**; **Jervan, Gert**; **Hollstein, Thomas**; **Raik, Jaan** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 83-86 : ill

Fast and optimized task allocation method for low vertical link density 3-Dimensional Networks-on-Chip based many core systems
Ying, Haoyuan; **Hollstein, Thomas**; Hofmann, Klaus Proceedings : Design, Automation & Test in Europe : Grenoble, France, March 18-22, 2013 2013 / p. 1777-1782 : ill

Fast data sort based on searching networks with ring pipeline
Sklyarov, Valery; Skliarova, Iouliia; **Sudnitsõn, Aleksander** Elektronika ir elektrotechnika = Electronics and electrical engineering 2016 / p. 58-62 : ill http://dx.doi.org/10.5755/j01.eie.22.4.15920

Fast matrix covering in all programmable systems-on-chip
Sklyarov, Valery; Skliarova, Iouliia; **Rjabov, Artjom**; **Sudnitsõn, Aleksander** Elektronika ir elektrotechnika = Electronics and electrical engineering 2014 / p. 150-153 : ill

Fault-resilient NoC router with transparent resource allocation
Putkaradze, Tsotne; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Raik, Jaan**; **Jervan, Gert** 12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC2017), July 12-14, 2017, Madrid, Spain : proceedings 2017 / 8 p. : ill https://doi.org/10.1109/ReCoSoC.2017.8016161 https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8016161

Fault-tolerant scheduling of mixed-critical applications on multi-processor platforms
Bagheri, Mehrdad; **Jervan, Gert** 2014 International Conference on Embedded and Ubiquitous Computing : EUC 2014 : 26-28 August 2014, Milano, Italy : proceedings 2014 / p. 25-32 : ill

Four years of System-on-Chip curricula
Kruus, Margus; **Ellervee, Peeter** EWME 2006 proceedings : 6th International Workshop on Microelectronics Education : 8-9 June, 2006, Stockholm, Sweden 2006 / p. 88-91

A framework for area-efficient concurrent online checkers design
Saltarelli, Pietro; **Niazmand, Behrad**; **Hariharan, Ranganathan**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 64-69 : ill

A framework for combining concurrent checking and online embedded test for low-latency fault detection in NoC routers
Saltarelli, Pietro; **Niazmand, Behrad**; **Raik, Jaan**; **Govind, Vineeth**; **Hollstein, Thomas**; **Jervan, Gert**; **Hariharan, Ranganathan** NOCS '15 : International Symposium on Networks-on-Chip : Vancouver, BC, Canada, September 28-30, 2015 2015 / [8] p. : ill http://dx.doi.org/10.1145/2786572.2788713

A framework for comprehensive automated evaluation of concurrent online checkers

Saltarelli, Pietro; **Niazmand, Behrad**; **Raik, Jaan**; **Hariharan, Ranganathan**; **Jervan, Gert**; **Hollstein, Thomas** Euromicro Conference on Digital System Design : DSD 2015 : 26-28 August 2015, Funchal, Madeira, Portugal : proceedings 2015 / p. 288-292 : ill http://dx.doi.org/10.1109/DSD.2015.15

From online fault detection to fault management in network-on-chips : a ground-up approach
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Janson, Karl**; **Nevin, George**; **Oyeniran, Adeboye Stephen**; **Putkaradze, Tsotne**; **Apneet Kaur**; **Raik, Jaan**; **Jervan, Gert**; **Ubar, Raimund-Johannes**; **Hollstein, Thomas** Proceedings 2017 IEEE 20th International Symposium on Design and Diagnotics of Electronic Circuit & Systems(DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 48-53 : ill https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553

Generalization of network-on-chip communication modelling
Ellervee, Peeter; **Tagel, Mihkel**; **Jervan, Gert** Workshop Digest. Diagnostic Services in Network-on-Chips - Test, Debug, and On-Line Monitoring : DATE 2009 : Nice, France, 20-24 April, 2009 2009 / ? p

GSNoC — the comprehensive design platform for 3-dimensional Networks-on-Chip based many core embedded systems
Ying, Haoyuan; **Hollstein, Thomas**; Hofmann, Klaus Proceedings of the 2013 International Conference on High Performance Computing & Simulation (HPCS 2013) : July 1-July 5, 2013, Helsinki, Finland 2013 / p. 217-223 : ill

Handling of SETs on NoC links by exploitation of inherent redundancy in circular input buffers [Online resource]
Janson, Karl; **Pihlak, Rene**; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Jervan, Gert**; **Raik, Jaan** BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p.: ill https://doi.org/10.1109/BEC.2018.8600989

A hardware/software co-design reconfigurable network-on-chip FPGA emulation method
Ying, Haoyuan; **Hollstein, Thomas**; Hofmann, Klaus 2014 9th International Symposium on Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC) : Montpellier, France, 26-28 May, 2014 2014 / [8] p. : ill

A hierarchical approach for devising area efficient concurrent online checkers
Niazmand, Behrad; **Azad, Siavoosh Payandeh**; **Ghasempouri, Tara**; **Raik, Jaan**; **Jervan, Gert** Proceedings 2nd IEEE International Test Conference in Asia : ITC-Asia 2018, 15-17 August 2018, Harbin, China 2018 / p. 139-144 : ill https://doi.org/10.1109/ITC-Asia.2018.00034

High-level modeling and testing of multiple control faults in digital systems
Jasnetski, Artjom; **Oyeniran, Adeboye Stephen**; **Tšertov, Anton**; Schölzel, Mario; **Ubar, Raimund-Johannes** Formal proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 20-22, 2016, Košice, Slovakia 2016 / [6] p. : ill http://dx.doi.org/10.1109/DDECS.2016.7482445

High-performance information processing in distributed computing systems
Sklyarov, Valery; **Rjabov, Artjom**; Skliarova, Iouliia; **Sudnitsõn, Aleksander** International journal of innovative computing, information and control 2016 / p. 139-160 : ill

Holistic approach for Fault-Tolerant Network-on-Chip based many-core systems [Online resource]
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** arXiv.org 2016 / [8] p. : ill

Hybrid BIST energy minimisation technique for system-on-chip testing
Jervan, Gert; **Peng, Zebo**; **Shchenova, Tatjana**; Ubar, Raimund-Johannes IEE proceedings computers & digital techniques 2006 / 4, p. 208-216 : ill https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=5ae755d323ccba87f8ff886334e3dd6d33560874

Interactions of Zynq-7000 devices with general purpose computers through PCI-express : a case study [Electronic resource]
Rjabov, Artjom; **Sudnitsõn, Aleksander**; Sklyarov, Valery; Skliarova, Iouliia Proceedings of the 18th Mediterranean Electrotechnical Conference MELECON 2016 : 18-20 April 2016, Limassol, Cyprus 2016 / [4] p. : ill. [CD-ROM] https://doi.org/10.1109/MELCON.2016.7495400

Kiipvõrgud - uus kiipsüsteemide projekteerimise paradigma
Tagel, Mihkel A & A 2006 / 5, lk. 33-42 : ill

Kognitiivelektroonika on elektroonika tulevik
Maidla, Margus Sirp 2016 / lk. 34-35 : fot http://www.sirp.ee/s1-artiklid/c21-teadus/kognitiivelektroonika-on-elektroonika-tulevik/

Kuidas testida arvutivõrku ränikiibil
Raik, Jaan; **Govind, Vineeth** A & A 2010 / 4, lk. 35-37 https://artiklid.elnet.ee/record=b2286479*est

LiD-CAT: A lightweight detector for cache ATtacks
Reinbrecht, Cezar; Hamdioui, Said; Taouil, Mottaqiallah; **Niazmand, Behrad**; **Ghasempouri, Tara**; **Raik, Jaan**; Sepulveda, Johanna 2020 IEEE European Test Symposium (ETS) : ETS 2020, May 25-29, 2020 Tallinn, Estonia : proceedings 2020 / 6 p. : ill

https://doi.org/10.1109/ETS48528.2020.9131603

Lightweight monitoring scheme for flooding DoS Attack detection in multi-tenant MPSoCs
Chaves Arroyave, Cesar Giovanni; Sepulveda, Johanna; **Hollstein, Thomas** 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea May 22-28, 2021 : proceedings 2021 / 5 p https://doi.org/10.1109/ISCAS51556.2021.9401153 Conference Proceedings at Scopus Article at Scopus Article at WOS

Logic-based implementation of fault-tolerant routing in 3D Network-on-Chips
Niazmand, Behrad; **Azad, Siavoosh Payandeh**; Flich, Jose; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 2016 Tenth IEEE/ACM International Symposium on Networks-on-Chip (NOCS) : Nara, Japan, 31 August - 2 September 2016 2016 / [8] p. : ill https://doi.org/10.1109/NOCS.2016.7579317

A method for crosstalk fault detection in on-chip buses
Bengtsson, Tomas; **Jutman, Artur**; **Ubar, Raimund-Johannes**; Kumar, Shashi Norchip : proceedings : Oulu, Finland, 21-22 November 2005 2005 / p. 285-288 : ill https://doi.org/10.1109/NORCHP.2005.1597045

Multi-view modeling for MPSoC design aspects [Online resource]
Vain, Jüri; **Apneet Kaur**; **Tsiopoulos, Leonidas**; **Raik, Jaan**; **Jenihhin, Maksim** BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p.: ill https://doi.org/10.1109/BEC.2018.8600986

Network-on-Chip with equality-of-service : a local fair runtime arbitration method for global fair bandwidth share
Samman, Faizal; **Hollstein, Thomas** International journal of innovative computing, information and control 2019 / p. 1821−1834 http://www.ijicic.net/servlet/Download?contentID=CONT34590d01977b424ea4f1cdfbb4c8c264 https://doi.org/10.24507/ijicic.15.05.1821 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

NOC mapping and scheduling
Nikiforov, Deniss Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 73-78 : ill

NoCDepend : a flexible and scalable dependability technique for 3D networks-on-chip
Hollstein, Thomas; **Azad, Siavoosh Payandeh**; **Kogge, Thilo**; Ying, Haoyuan; Hofmann, Klaus 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 75-78 : ill http://dx.doi.org/10.1109/DDECS.2015.30

Pipelined execution of data-parallel algorithms
Gorev, Maksim; **Ubar, Raimund-Johannes** BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 109-112 : ill

Processing sorted subsets in a multi-level reconfigurable computing system
Rjabov, Artjom; Sklyarov, Valery; Skliarova, Iouliia; **Sudnitsõn, Aleksander** Elektronika ir elektrotechnika = Electronics and electrical engineering 2015 / p. 30-33 : ill http://dx.doi.org/10.5755/j01.eee.21.2.11509

QoSinNoC: analysis of QoS-aware NoC architectures for mixed-criticality applications
Avramenko, Serhiy; **Azad, Siavoosh Payandeh**; **Niazmand, Behrad**; **Raik, Jaan**; **Jenihhin, Maksim** 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 67-72 : ill https://doi.org/10.1109/DDECS.2018.00-10

Review, analysis, and implementation of path selection strategies for 2D NoCs
Singh, Rajendra; Bohra, Manoj Kumar; Hemrajani, Prashant; Kalla, Anshuman; Bhatt, Devershi Pallavi; Purohit, Nitin; **Daneshtalab, Masoud** IEEE Access 2022 / p. 129245 - 129268 https://doi.org/10.1109/ACCESS.2022.3227460 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Runtime contention and bandwidth-aware adaptive routing selection strategies for networks-on-chip
Samman, Faizal; **Hollstein, Thomas**; Glesner, Manfred IEEE transactions on parallel and distributed systems 2013 / p. 1411-1421 : ill

SOC at smart home realizations
Kuusik, Alar Raadiotehnika 2001 : VIII rahvusvahelise telekommunikatsioonipäeva materjalid 2001 / lk. 121-122

SoCDep2 : a framework for dependable task deployment on many-core systems under mixed-criticality constraints
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Ellervee, Peeter**; **Raik, Jaan**; **Jervan, Gert**; **Hollstein, Thomas** 2016 11th International Symposium on Reconfigurable Communication‐centric Systems‐on‐Chip (ReCoSoC) : June 27‐29, 2016, Tallinn, Estonia 2016 / [6] p. : ill https://doi.org/10.1109/ReCoSoC.2016.7533903

Split-chip design to prevent IP reverse engineering
Pagliarini, Samuel Nascimento; Sweeney, Joseph; Mai, Ken; Blanton, Shawn; Mitra, Subhasish; Pileggi, Larry IEEE Design and Test 2020 / p. 109-118 https://doi.org/10.1109/MDAT.2020.3033255 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Synthesis of multiple fault oriented test groups from single fault test sets [Electronic resource]
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** 2013 8th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS) : 26-28 March 2013, Abu Dhabi, UAE 2013 / p. 36-41 : ill [CD-ROM]

System level design of dependable real-time Systems-on-Chip
Tagel, Mihkel; **Jervan, Gert** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 77-80 : ill

System-level communication synthesis and dependability improvements for Network-on-Chip based systems
Tagel, Mihkel; **Ellervee, Peeter**; **Jervan, Gert** Estonian journal of engineering 2010 / 1, p. 23-38 : ill https://artiklid.elnet.ee/record=b1964968*est

System-level design of timing-sensitive network-on-chip based dependable systems = Kiipvõrkudel põhinevate ajakriitiliste ja töökindlate süsteemide kõrgtaseme disain
Tagel, Mihkel 2012 https://www.ester.ee/record=b2778263*est

System-level optimization of NoC-based timing sensitive systems
Tagel, Mihkel; **Ellervee, Peeter**; **Hollstein, Thomas**; **Jervan, Gert** Estonian journal of engineering 2011 / 2, p. 158-168 : ill https://artiklid.elnet.ee/record=b2422982*est

zamiaCAD : understand, develop and debug hardware designs
Jenihhin, Maksim; **Tihhomirov, Valentin**; **Saif Abrar, Syed**; **Raik, Jaan**; Bartsch, Günter DUHDe : 1st Workshop on Design Automation for Understanding Hardware Designs : March 28, 2014 : Friday Workshop at DATE 2014, Dresden, Germany 2014 / p. 1-6

Zynq-based system for extracting sorted subsets from large data sets
Sklyarov, Valery; Skliarova, Iouliia; **Rjabov, Artjom**; **Sudnitsõn, Aleksander** Journal of microelectronics, electronic components and materials 2015 / p. 142-152 : ill

Techniques for robust routing, communication and computation in multiprocessor systems = Robustse marsruutimise, side ja arvutuse tehnikad mitmeprotsessorilistes süsteemides
Janson, Karl 2021 https://www.ester.ee/record=b5396084*est https://digikogu.taltech.ee/et/Item/c9091d5c-dcd8-4b21-95a7-84ead85241e6 https://doi.org/10.23658/taltech.3/2021

2018 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC) : 30-31 October 2018, Tallinn, Estonia : proceedings in IEEE Xplore [Online resource]
2018 https://ieeexplore.ieee.org/xpl/conhome/8552599/proceeding

2019 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC), 29-30 October 2019, Helsinki, Finland : proceedings in IEEE Xplore
2019

Upgrading QoSinNoC : efficient routing for mixed-criticality applications and power analysis
Avramenko, Serhiy; **Azad, Siavoosh Payandeh**; Violante, Massimo; Niazmand, Behrad; **Raik, Jaan**; **Jenihhin, Maksim** Proceedings of the 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 8-10, 2018, Verona, Italy 2018 / p. 207-212 : ill https://doi.org/10.1109/VLSI-SoC.2018.8644866