

Automated design error debug using high-level decision diagrams and mutation operators

Raik, Jaan; Repinski, Urmaz; Tšepurov, Anton; Hantson, Hanno; Ubar, Raimund-Johannes; Jenihhin, Maksim

Microprocessors and microsystems 2013 / p. 505-513 : ill

Fast RTL fault simulation using decision diagrams and bitwise set operations

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes; Ellervee, Peeter 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 3-5 October 2011, Vancouver, Canada 2011 / p. 164-170

<https://ieeexplore.ieee.org/document/6104440>

High-level modeling and testing of multiple control faults in digital systems

Jasnetski, Artjom; Oyeniran, Adeboye Stephen; Tšertov, Anton; Schölzel, Mario; Ubar, Raimund-Johannes Formal proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 20-22, 2016, Košice, Slovakia 2016 / [6] p. : ill <http://dx.doi.org/10.1109/DDECS.2016.7482445>

Laboratory framework TEAM for investigating the dependability issues of microprocessor systems

Jasnetski, Artjom; Tšertov, Anton; Ubar, Raimund-Johannes; Kruus, Helena 10th European Workshop on Microelectronics Education : EWME 2014 : May 14-16, 2014, Tallinn, Estonia 2014 / p. 80-83 : ill

Minimization of the high-level fault model for microprocessor control parts [Online resource]

Ubar, Raimund-Johannes; Oyeniran, Adeboye Stephen; Medaiyese, Olusiji BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p.: ill

<https://doi.org/10.1109/BEC.2018.8600980>

New fault models and self-test generation for microprocessors using High-Level Decision Diagrams

Jasnetski, Artjom; Raik, Jaan; Tšertov, Anton; Ubar, Raimund-Johannes 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 251-254 : ill

On automatic software-based self-test program generation based on high-Level decision diagrams

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 177 <http://dx.doi.org/10.1109/LATW.2016.7483357>

Software-based self-test generation for microprocessors with high-level decision diagrams

Ubar, Raimund-Johannes; Tšertov, Anton; Jasnetski, Artjom; Brik, Marina LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Software-based self-test generation for microprocessors with high-level decision diagrams

Jasnetski, Artjom; Ubar, Raimund-Johannes; Tšertov, Anton; Brik, Marina Proceedings of the Estonian Academy of Sciences 2014 / p. 48-61 : ill https://artiklid.elnet.ee/record=b2665215*est