

### **Abstraction of clock interface for conversion of RTL VHDL to SystemC**

**Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan** 2014 IEEE International Advance Computing Conference (IACC) : February 21-22, 2014, Gurgaon, India 2014 / p. 50-55 : ill

### **Application specific processor synthesis from assembler code using VHDL**

**Udre, Jüri** Asian-Pacific Conference on Hardware Description Languages, Standards and Applications CAPCHDLA-93, Australia 1993

### **Application specific processor synthesis from assembler code using VHDL**

**Tammemäe, Kalle; Udre, Jüri; Wehn, N.; Gasteier, M.; Glesner, M.** APCHDLA-93 Dec. 6-9, 1993 1993

### **Compaction of decision diagrams for describing multi-process VHDL descriptions**

**Leveugle, R.; Saucier, Gabriele; Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 195-198: ill

### **Comprehensive abstraction of VHDL RTL cores to ESL SystemC = Register-siirde taseme VHDL kirjelduste kompleksne abstraherimine süsteemitaseme SystemC mudeliteks**

**Abrar, Syed Saif** 2016 [http://www.ester.ee/record=b4564850\\*est](http://www.ester.ee/record=b4564850*est)

### **EEG analyzer prototype based on FPGA**

**Jenihhin, Maksim; Gorev, Maksim; Pesonen, Vadim; Mihailov, Dmitri; Ellervee, Peeter; Hinrikus, Hiie; Bachmann, Maie; Lass, Jaanus** 7th International Symposium on Image and Signal Processing and Analysis (ISPA 2011) : September 4-6, 2011, Dubrovnik, Croatia : proceedings 2011 / p. 101-106 : ill <https://ieeexplore.ieee.org/document/6046588>

### **Extensible open-source framework for translating RTL VHDL IP cores to SystemC**

**Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan** Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

### **Formalization and validation of the std logic-1164 and numeric-std VHDL packages using the nqthm theorem prover**

**Dušina, Julia; Borriane, Dominique** 2nd Workshop on Libraries, Component Modeling and Quality Assurance : proceedings : Toledo, Spain, April, 1997 1997 / p. 169-180

### **Implementation-independent macro-library for telecommunication in VHDL**

**Khan, Mozammel H.; Hemani, Ahmed; Tenhunen, Hannu** BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 291-294: ill

### **Improved VHDL input for high-level synthesis tool xTractor**

**Ellervee, Peeter; Ivask, Eero; Kruus, Margus** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 87-90 : ill

### **Integration of digital test tools to the internet-based environment MOSCITO**

**Schneider, Andre; Diener, Karl-Heinz; Elst, Günter; Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes** SCI 2003 : the 7th World Multiconference on Systemics, Cybernetics and Informatics : July 27-30, 2003, Orlando, Florida, USA : proceedings. Volume VIII, Applications of Informatics and Cybernetics in Science and Engineering 2003 / p. 136-141 : ill  
[https://www.researchgate.net/publication/250063424\\_Integration\\_of\\_Digital\\_Test\\_Tools\\_to\\_the\\_Internet-Based\\_Environment\\_MOSCITO](https://www.researchgate.net/publication/250063424_Integration_of_Digital_Test_Tools_to_the_Internet-Based_Environment_MOSCITO)

### **Kas VHDL on sobiv keel sünteesiks?**

**Tammemäe, Kalle** Arvutustehnika ja Andmetöötlus 1995 / 7, lk. 2-7; 8, lk. 8-14

### **Localization of bugs in processor designs using zamiaCAD framework**

**Tšepurov, Anton; Tihomirov, Valentin; Jenihhin, Maksim; Raik, Jaan** 13th International Workshop on Microprocessor Test and Verification (MTV 2012) Common Challenges and Solutions : Austin, USA, December 10-12, 2012 2012 / p. 1-6  
<https://ieeexplore.ieee.org/document/6519733>

### **Model synthesis from VHDL for the functional test generation system**

**Krupnova, Helena** 1993 [https://www.ester.ee/record=b2090509\\*est](https://www.ester.ee/record=b2090509*est)

### **Optimization methodologies for Cycle-Accurate SystemC models converted from RTL VHDL**

**Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan** IP-SoC 2013 : IP embedded system conference and exhibition : Grenoble, France, November 6-7, 2013 2013

### **Performance analysis of cosimulating processor core in VHDL and SystemC**

**Saif Abrar, Syed; Shyam Kiran A.; Jenihhin, Maksim; Raik, Jaan; Babu, C.** Proceedings of the 2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 22-25 August 2013, Mysore, India 2013 / p. 563-568 : ill

### **Riistvara kirjeldamise keel VHDL**

**Tammemäe, Kalle** Arvutustehnika ja Andmetöötlus 1992 / 4, lk. 1-11: ill

### **Riistvara kirjeldamiskeel - VHDL : metoodiline materjal**

1992 [https://www.ester.ee/record=b1062926\\*est](https://www.ester.ee/record=b1062926*est)

### **Riistvara kirjeldamiskeel - VHDL : metoodiline materjal**

**Tammemäe, Kalle** 2003 [http://www.ester.ee/record=b1605950\\*est](http://www.ester.ee/record=b1605950*est)

### **Riistvara kirjeldamiskeel VHDL : metoodiline materjal**

**Tammemäe, Kalle** 2002 [http://www.ester.ee/record=b1605950\\*est](http://www.ester.ee/record=b1605950*est)

### **Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation**

Leveugle, R.; **Ubar, Raimund-Johannes** Electron technology 1999 / 3, p. 282-287 : ill

### **Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation**

Leveugle, R.; **Ubar, Raimund-Johannes** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 353-358 <https://hal.science/ccsd-00015077/>

### **Test pattern generation at the behavioral level from VHDL circuit description containing several processes**

Gramatova, Elena; Bezakova, Jana; Cibakova, Tatiana BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 145-148

### **Transforming VHDL descriptions from behavior to structure**

**Berkman, Boriss; Sudnitsõn, Aleksander; Udre, Jüri** Tallinna Tehnikaülikooli Toimetised 1990 / lk. 27-44: ill

### **Translating behavioral VHDL for emulation**

**Ellervee, Peeter; Reinsalu, Uljana; Arhipov, Anton** 25th IEEE NORCHIP Conference : Aalborg, Denmark, 19-20 November 2007 2007 / ? p <https://ieeexplore.ieee.org/document/4481073>

### **VHDL based test generation system**

**Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 5th Electronic Devices and Systems Conference, Brno, June 11-12, 1998 1998 / p. 145-148

### **VHDL design debug framework based on zamiaCAD**

**Tihhomirov, Valentin; Tšepurov, Anton; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan** DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill

### **VHDL front-end for high-level synthesis tool xTractor**

**Ivask, Eero; Ellervee, Peeter** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 111-114 : ill

### **VHDL täna ja homme**

**Tammemäe, Kalle** Arvutustehnika ja Andmetöötlus 1993 / 9, lk. 1-8

### **VLSI kõrgtaseme süntees**

**Tammemäe, Kalle** Arvutustehnika ja Andmetöötlus 1993 / 1, lk. 25-31