

**Extended checkers for control part of routers in network-on-chips**

**Hariharan, Ranganathan; Niazmand, Behrad; Hollstein, Thomas; Raik, Jaan; Jervan, Gert** MEDIAN 2015 : the 4th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : March 13, 2015, Grenoble, France 2015 / p. 36-39 : ill

**Gate-level graph representation learning : a step towards the improved stuck-at faults analysis**

**Balakrishnan, Aneesh; Alexandrescu, Dan; Jenihhin, Maksim; Lange, Thomas; Glorieux, Maximilien** Proceedings of the Twenty Second International Symposium on Quality Electronic Design (ISQED) : Santa Clara, USA, 7-9 April 2021 2021 / p. 24-30  
<https://doi.org/10.1109/ISQED51717.2021.9424256>

**A hierarchical approach for devising area efficient concurrent online checkers**

**Niazmand, Behrad; Azad, Siavoosh Payandeh; Ghasempouri, Tara; Raik, Jaan; Jervan, Gert** Proceedings 2nd IEEE International Test Conference in Asia : ITC-Asia 2018, 15-17 August 2018, Harbin, China 2018 / p. 139-144 : ill  
<https://doi.org/10.1109/ITC-Asia.2018.00034>

**Mixed-level identification of fault redundancy in microprocessors**

**Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Gürsoy, Cemil Cem; Raik, Jaan** LATS 2019 : 20th IEEE Latin American Test Symposium : Santiago, Chile, March 11th - 13th 2019 2019 / 6 p. : ill  
<https://doi.org/10.1109/LATW.2019.8704591>