

Bringing research issues into lab scenarios on the example of SoC testing [Electronic resource]
Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei; Wuttke, Heinz-Dietrich International Conference on Engineering Education - ICEE 2007 : September 3-7, 2007, Coimbra, Portugal 2007 / [7] p. : ill. [CD-ROM]
<http://icee2007.dei.uc.pt/proceedings/papers/429.pdf>

High-level modeling and testing of multiple control faults in digital systems
Jasnetski, Artjom; Oyeniran, Adeboye Stephen; Tšertov, Anton; Schölzel, Mario; Ubar, Raimund-Johannes Formal proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 20-22, 2016, Košice, Slovakia 2016 / [6] p. : ill <http://dx.doi.org/10.1109/DDECS.2016.7482445>

How to generate high quality tests for digital systems
Ubar, Raimund-Johannes; Aarna, Margit; Kruus, Helena; Raik, Jaan 2004 International Semiconductor Conference : 27th edition, October 4-6, 2004, Sinaia, Romania : CAS 2004 proceedings. Volume 2 2004 / p. 459-462 : ill
<http://dx.doi.org/10.1109/SMICND.2004.1403048>

Multiple control fault testing in digital systems with high-level decision diagrams
Ubar, Raimund-Johannes; Oyeniran, Adeboye Stephen 2016 IEEE International Conference on Automation, Quality and Testing, Robotics (AQTR) : THETA 20th edition : 19th-21st May, Cluj-Napoca, Romania : proceedings 2016 / [6] p. : ill
<http://dx.doi.org/10.1109/AQTR.2016.7501287>

Multiple fault testing in systems-on-chip with high-level decision diagrams
Ubar, Raimund-Johannes; Oyeniran, Adeboye Stephen; Schölzel, Mario; Vierhaus, Heinrich Theodor Proceedings of 2015 10th International Design & Test Symposium (IDT) : Dead Sea, Jordan, 14-16 December 2015 2015 / p. 66-71 : ill
<http://dx.doi.org/10.1109/IDT.2015.7396738>

SCAAT: Secure cache alternative address table for mitigating cache logical side-channel attacks
Shalabi, Amer; Ghasempouri, Tara; Ellervee, Peeter; Raik, Jaan 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / art, 20035366, p. 213-217 <https://doi.org/10.1109/DSD51259.2020.00043>

Synthesis of high-level decision diagrams for functional test pattern generation
Ubar, Raimund-Johannes; Raik, Jaan; Karputkin, Anton; Tombak, Mati Proceedings of the 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009 : Lodz, Poland, 25-27 June, 2009 2009 / p. 519-524 : ill