

Acceleration of recursive data sorting over tree-based structures

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Sklyarov, Valery; Skliarova, Iuliia Elektronika ir elektrotehnika = Electronics and electrical engineering 2011 / p. 51-56 : ill <https://eejournal.ktu.lt/index.php/elt/article/view/612>

Algorithms of functional level testability analysis for digital circuits

Ubar, Raimund-Johannes; Kuchcinski, Ktysztof Periodica polytechnica. Electrical engineering 1992 / 3/4, p. 295-308

Approaches to improve hierarchical ATPG for synchronous sequential circuits

Viilukas, Taavi Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kuuenda aastakonverentsi artiklite kogumik : 3.-5. oktoobril 2012, Laulasmaa 2012 / p. 105-108 : ill

Automated test pattern generator with constraint solver

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 33-36

Automatic synthesis of asynchronous circuits from synchronous RTL descriptions

Öberg, Johnny; Plosila, Juha; Ellervee, Peeter Proceedings 23rd NORCHIP Conference : Oulu, Finland, 21-22 November 2005 2005 / p. 200-205 : ill <https://ieeexplore.ieee.org/document/1597024/keywords#keywords>

Back-traced deductive-parallel fault simulation for digital systems

Hahanov, Vladimir; Ubar, Raimund-Johannes; Hyduke, Stanley Proceedings : Euromicro Symposium on Digital System Design : Belek-Antalya, Turkey, September 1st to 6th, 2003 2003 / p. 370-377 : ill <https://ieeexplore.ieee.org/document/1231969>

Boolean fault diagnosis with structurally synthesized BDDs

Ubar, Raimund-Johannes Recent progress in the Boolean domain 2014 / p. 303-331 : ill

Code coverage analysis for concurrent programming languages using high-level decision diagrams

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes Proceedings of the 12th European Workshop on Dependable Computing : EWDC 2009 : Toulouse, France, May 14-15, 2009 2009 / [4] p. : ill <https://hal.archives-ouvertes.fr/hal-00381559>

Collaborative distributed computing in the field of digital electronics testing

Ivask, Eero; Devadze, Sergei; Ubar, Raimund-Johannes Balanced Automation Systems for Future Manufacturing Networks : 9th IFIP WG 5.5 International Conference : BASYS 2010 : Valencia, Spain, July 21-23, 2010 : proceedings 2010 / p. 145-152

Collaborative distributed fault simulation for digital electronic circuits

Ivask, Eero; Devadze, Sergei; Ubar, Raimund-Johannes Intelligent Distributed Computing IV : proceedings of the 4th International Symposium on Intelligent Distributed Computing - IDC 2010 : Tangier, Morocco, September 2010 2010 / p. 67-76

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Raik, Jaan; Rannaste, Anna; Jenihhin, Maksim; Viilukas, Taavi; Ubar, Raimund-Johannes; Fujiwara, Hideo Sixteenth IEEE European Test Symposium : 23-27 May 2011, Trondheim 2011 / p. 147-152

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Viilukas, Taavi; Raik, Jaan; Ubar, Raimund-Johannes; Rannaste, Anna; Jenihhin, Maksim; Fujiwara, Hideo Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 139-142 : ill

Constraints solving based hierarchical test generation for synchronous sequential circuits = Kitsenduste lahendamisel baseeruv hierarhiline testigeneerimine sünkroonsetele järjestikskeemidele

Viilukas, Taavi 2012 https://www.ester.ee/record=b2888278*est

Decision diagrams for diagnostic modeling

Ubar, Raimund-Johannes MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 43

Defect-oriented modul-level fault diagnosis in digital circuits

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 81-86

Defect-oriented test- and layout-generation for standard-cell ASIC designs

Sudbrock, Joachim; Raik, Jaan; Ubar, Raimund-Johannes; Kuzmich, Wieslaw; Pleskacz, Witold A. Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 79-82 : ill <https://ieeexplore.ieee.org/document/1559781>

Description of digital objects with alternative graphs for test generation purposes

Ubar, Raimund-Johannes; Lohuaru, Tõnu Fault Tolerant Systems and Diagnostics : XI. International Conference ; Proceedings ; Suhl, June 6-9, 1988 1988 / p. [?]

Design and test technology for dependable systems-on-chip

2011 https://www.ester.ee/record=b4467408*est

Design error diagnosis using backtrace algorithm on decision diagrams

Repinski, Urmas; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim; Tšepurov, Anton Info- ja

kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

Design obfuscation versus test

Farahmandi, Farimah; Sinanoglu, Ozgur; Blanton, Ronald; **Pagliarini, Samuel Nascimento** 2020 IEEE European Test Symposium (ETS) : ETS 2020, May 25 - 29, 2020, Tallinn, Estonia 2020 / 10 p <https://doi.org/10.1109/ETS48528.2020.9131590>

Design of FPGA-based circuits using hierarchical finite state machines

Skliarova, Iuliia; Sklyarov, Valery; **Sudnitsõn, Aleksander** 2012 http://www.ester.ee/record=b2857138*est

Design-aid programs for LSI integrated circuits

Tarnay, K.; Szekely, V.; Baji, P.; Farkas, G.; Masszi, F.; Kerecsen-Rencz, M. Проблемы моделирования и измерения в электронике 1986 / p. 3-11

DFT-based external test and diagnosis of mesh-like networks on chips = Testitavusel põhinev välise testi ja diagnoosi meetod kahemõõtmelistele kiipvõrkudele

Govind, Vineeth 2009 <https://digi.lib.ttu.ee/i/?454> https://www.ester.ee/record=b2539211*est

Digital test in WEB-based environment

Ivask, Eero 2006 https://www.ester.ee/record=b2158119*est

Dynamic analysis of digital circuits with multi-valued simulation

Ubar, Raimund-Johannes Microelectronics journal 1998 / 11, p. 821-826: ill

Evolutionary two-criteria optimization of finite state machines

Spitšakova, Margarita Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 101-104

Evolutionary approach to the functional test generation for digital circuits

Skobtsov, Y.A.; Ivanov, D.E.; Skobtsov, V.Y.; **Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 229-232 : ill

Fast fault emulation for synchronous sequential circuits

Raik, Jaan; Ellervee, Peeter; Tihomirov, Valentin; **Ubar, Raimund-Johannes** Proceedings of East-West Design & Test Workshop (EWDTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 35-40
<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=a6eb712498a5f23db3f95ad66bada257c21e96f0>

Fast fault simulation for extended class of faults in scan-path circuits

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur Proceedings : Fifth IEEE International Symposium on Electronic Design, Test and Applications : DELTA 2010 : 13-15 January 2010, Ho Chi Minh City, Vietnam 2010 / p. 14-19
<https://ieeexplore.ieee.org/document/5438717>

Fault collapsing in digital circuits using fast fault dominance and equivalence analysis with SSBDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; Orasson, Elmet; Raik, Jaan VLSI-SoC : Design for Reliability, Security, and Low Power : 23rd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2015 Daejeon, Korea, October 5-7, 2015 : revised selected papers 2016 / p. 23-45 : ill https://doi.org/10.1007/978-3-319-46097-0_2 [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Fault simulation of digital systems = Digitaalsüsteemide rikete simuleerimine

Devadze, Sergei 2009 <https://digi.lib.ttu.ee/i/?445> https://www.ester.ee/record=b2508727*est

Finite state machine synthesis for low power using input-disabling precomputation architectures

Sudnitsõn, Aleksander The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 137-140 : ill

FPGA implementation of the polynomial curve fitting

Gorev, Maksim; Pesonen, Vadim Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite

FPGA-based fault emulation of synchronous sequential circuits

Ellervee, Peeter; Raik, Jaan; Tammemäe, Kalle; Ubar, Raimund-Johannes IET computers and digital techniques 2007 / 2, p. 70-76 : ill <https://ieeexplore.ieee.org/abstract/document/1423822>

FPGA-based implementation of EEG analyzer

Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Jenihhin, Maksim; Ellervee, Peeter DATE'11 Friday Workshop on "Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing" : Grenoble, France, March 2011 2011 / [1] p <https://www.microsoft.com/en-us/research/wp-content/uploads/2017/03/ellervee.pdf>

FPGA-based systems in information and communication

Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander AICT2011 : 5th International Conference on Application of Information and Communication Technologies : 12-14 October, Baku, Azerbaijan : conference proceedings 2011 / p. 551-555 https://www.researchgate.net/publication/254014990_FPGA-based_systems_in_information_and_communication

Functional level controllability analysis for digital circuits

Ubar, Raimund-Johannes; Kuchcinski, Ktysztof Proc. of the Design Automation Conference, Kaunas, Lithuania, June 1-4, 1992 1992 / p. 13-21

Functional level testability analysis for digital circuits

Ubar, Raimund-Johannes 1992

Functional self-test of high-performance pipe-lined signal processing architectures

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart Microprocessors and microsystems 2015 / p. 909-918 : ill <https://doi.org/10.1016/j.micpro.2014.11.002> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Hierarchical defect-oriented fault simulation for digital circuits

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmich, W.; Lobur, M.; Pleskacz, Witold A.; Raik, Jaan; Ubar, Raimund-Johannes IEEE European Test Workshop : 23-26 May 2000, Cascais, Portugal : ETW 2000 : proceedings 2000 / p. 69-74 : ill <https://ieeexplore.ieee.org/document/873781>

Hierarchical fault simulation for finite state machines

Brik, Marina; Raik, Jaan; Ubar, Raimund-Johannes The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 145-148 : ill

Hierarchical test generation for digital circuits represented by Decision Diagrams : thesis on informatics and system engineering

Raik, Jaan 2001 https://www.ester.ee/record=b1578107*est

Hierarchical test pattern generation and untestability identification techniques for synchronous sequential circuits =

Hierarhilised testintegreerimise ja mittetestitavuse identifitseerimise meetodid sünkroonsetele järjestikskeskemidele
Rannaste, Anna 2010 https://www.ester.ee/record=b2637391*est

Hierarhilisest testigeneerimisest ja mittetestitavuse analüüsist

Rannaste, Anna A & A 2010 / 4, lk. 38-39 https://artiklid.elnet.ee/record=b2286481*est

High-level decision diagrams based coverage metrics for verification and test

Jenihhin, Maksim; Raik, Jaan; Tšepurov, Anton; Reinsalu, Uljana; Ubar, Raimund-Johannes LATW 2009 : 10th IEEE Latin American Test Workshop : Buzios, Rio de Janeiro, Brazil, March 2-5, 2009 2009 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2009.4813792>

Hybrid built-in self-test : methods and tools for analysis and optimization of BIST = Sisseehitatud hübriidne isetestimine : meetodid ja vahendid analüüsiks ning optimeerimiseks

Orasson, Elmet 2007 https://www.ester.ee/record=b2305436*est

Improved fault emulation for synchronous sequential circuits

Raik, Jaan; Ellervee, Peeter; Tihhomirov, Valentin; Ubar, Raimund-Johannes Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 72-78 : ill

Improved testability calculation for digital circuits

Ubar, Raimund-Johannes; Heinlaid, J.; Raun, L. 19th NORCHIP Conference, Kista, Sweden, 12-13 November 2001 : proceedings 2001 / p. 264-270 : ill

Increasing the speed of delay simulation in digital circuits

Ubar, Raimund-Johannes; Jutman, Artur The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 31-34 : ill

Investigation and development of test generation methods for control part of digital systems

Brik, Marina 2002 http://www.ester.ee/record=b1688656*est

LFSR polynomial and seed selection using genetic algorithm

Aleksejev, E.; Jutman, Artur; Ubar, Raimund-Johannes BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 179-182 : ill

Logic simulation and fault collapsing with shared structurally synthesized BDDs

Mironov, Dmitri; Ubar, Raimund-Johannes; Raik, Jaan 2014 19th IEEE European Test Symposium (ETS) : May 26th-30th, 2014, Paderborn, Germany : proceedings 2014 / [2] p. : ill

Lower bounds of the size of shared structurally synthesized BDDs

Ubar, Raimund-Johannes; Mironov, Dmitri Proceedings of the 2014 IEEE 17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 23-25, 2014, Warsaw, Poland 2014 / p. 77-82 : ill

Macro level defect-oriented diagnosability of digital circuits

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 149-152 : ill

Macro level defect-oriented diagnosability of digital circuits

Kostin, Sergei; Ubar, Raimund-Johannes; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 53-56 : ill

Mixed-level defect simulation in data-paths of digital systems

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 617-620 : ill <https://ieeexplore.ieee.org/document/1003333>

Modeling sequential circuits with shared structurally synthesized BDDs

Ubar, Raimund-Johannes; Marenkov, Mihhail; Mironov, Dmitri; Viies, Vladimir Proceedings of 2014 9th International Design & Test Symposium (IDT) : Sheraton Club des Pins Hotel, Algiers, Algeria, December 16-18, 2014 2014 / p. 130-135 : ill

Multi-level test generation and fault diagnosis for finite state machines

Ubar, Raimund-Johannes; Brik, Marina Dependable computing : proceedings / EDCC-2, Second European Dependable Computing Conference, Taormina, Italy, October 2-4, 1996 1996 / p. 264-281 : ill

Multi-level test generation and fault diagnosis in digital systems

Ubar, Raimund-Johannes 1992

Multi-valued simulation of digital circuits

Ubar, Raimund-Johannes Proceedings : 1997 21st International Conference on Microelectronics : Niš, Yugoslavia, 14-17 September 1997. Vol. 2 1997 / p. 721-724 : ill

New technique for hierarchical identification of untestable faults in sequential circuits

Krivenko, Anna; Ubar, Raimund-Johannes; Raik, Jaan; Kruus, Margus Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / lk. 155-158 : ill

A novel random approach to diagnostic test generation

Osimiry, Emmanuel Ovie; Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan 2nd IEEE NORCAS Conference : 1-2 November 2016, Copenhagen, Denmark 2016 / [4] p. : ill <https://doi.org/10.1109/NORCHIP.2016.7792915>

Optimization of built-in self-test in digital systems = Sisseehitatud enesetestimise optimeerimine digitaalsüsteemides

Kruus, Helena 2011

Overview of the modular system for inference of finite state machines

Spitšakova, Margarita Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 95-98 : ill

Parallel fault backtracing for calculation of fault coverage

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur 43rd International Conference on Microelectronics, Devices and Materials and the Workshop on Electronic Testing : September 12. - September 14.2007, Bled, Slovenia : MIDEM

conference 2007 proceedings 2007 / p. 165-170 : ill
https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel processing in FPGA-based digital circuits and systems

Sklyarov, Valery; Skliarova, Ioulia 2013 http://www.ester.ee/record=b2946103*est

Parallel X-fault simulation with critical path tracing technique [Electronic resource]

Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan; Jutman, Artur DATE 10 : Design, Automation & Test in Europe : Dresden, Germany, 8-12 March, 2010 2010 / p. 879-884 [CD-ROM] https://www.researchgate.net/publication/221341788_Parallel_X-fault_simulation_with_critical_path_tracing_technique

Practical works for on-line teaching design and test of digital circuits

Jutman, Artur; Ubar, Raimund-Johannes; Hahanov, V.; Skvortsova, O. The 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS 2002 : September 15-18, 2002, Dubrovnik, Croatia. Volume III 2002 / p. 1223-1226 : ill
<http://dx.doi.org/10.1109/ICECS.2002.1046474>

Recursion and hierarchy in digital design and prototyping : a case study

Mihailov, Dmitri; Kruus, Margus; Sklyarov, Valery; Skliarova, Ioulia; Sudnitsõn, Aleksander Computer Systems and Technologies : 12th International Conference, CompSysTech'11 : Vienna, Austria, June 16-17, 2011 : proceedings 2011 / p. 45-50 : ill
<https://dl.acm.org/doi/pdf/10.1145/2023607.2023616>

Representing logical inference steps with digital circuits

Matsak, Erika Human interface and the management of information : information and interaction 2009 / p. 178-184
https://link.springer.com/chapter/10.1007/978-3-642-02559-4_20

Research on digital system design and test at Tallinn University of Technology

Ubar, Raimund-Johannes; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert; Jutman, Artur; Kruus, Margus; Raik, Jaan Research in Estonia : present and future 2011 / p. 184-205 : ill

Riistvara kirjeldamiskeel - VHDL : metoodiline materjal

Tammemäe, Kalle 2003 http://www.ester.ee/record=b1605950*est

Riistvara kirjeldamiskeel VHDL : metoodiline materjal

Tammemäe, Kalle 2002 http://www.ester.ee/record=b1605950*est

Self-diagnosis in digital systems = Isediagnoosivad digitaalsüsteemid

Kostin, Sergei 2012 https://www.ester.ee/record=b2757857*est

Sequential circuits BIST synthesis from signal specifications

Raik, Jaan; Jenihhin, Maksim; Adelbert, Rain Proceedings 23rd NORCHIP Conference : Oulu, Finland, 21-22 November 2005 2005 / p. 196-199 : ill <https://ieeexplore.ieee.org/document/1597023>

Shared Structurally Synthesized BDDs for speeding-up parallel pattern simulation in digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Raik, Jaan 2015 Nordic Circuits and Systems Conference (NORCAS) : NORCHIP & International Symposium on System-on-Chip (SoC) : 1st IEEE NORCAS Conference : 26-28 October 2015, Oslo, Norway 2015 / [4] p. : ill <http://dx.doi.org/10.1109/NORCHIP.2015.7364406>

Sisseehitatud isetestimine digitaalsüsteemides

Kruus, Helena A & A 2011 / lk. 32-37 : ill https://artiklid.elnet.ee/record=b2472216*est

Structural fault collapsing by superposition of BDDs for test generation in digital circuits

Ubar, Raimund-Johannes; Mironov, Dmitri; Raik, Jaan; Jutman, Artur Proceedings of the Eleventh International Symposium on Quality Electronic Design ISQED 2010 : March 22-24, 2010 San Jose, California USA 2010 / p. 250-257 : ill
<https://ieeexplore.ieee.org/document/5450451>

Test program generation for microprocessor systems

Dušina, Julia 1993 https://www.ester.ee/record=b2090526*est

Testability calculation for digital circuits with decision diagrams

Ubar, Raimund-Johannes 3rd IEEE Latin American Test Workshop : LATW'02, Montevideo, Uruguay, February 10-13, 2002 : digest of papers 2002 / p. 137-143 : ill <https://dblp.org/rec/conf/latw/Ubar02.html>

Testability guided hierarchical test generation with decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Nõmmeots, Tanel 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 2002 / p. 265-271 <https://www.semanticscholar.org/paper/Testability-Guided-Hierarchical-Test-Generation-Ubar-Raik/c6301ac35d003c92f3867f26e2e75b87e1ad9b47>

Testing strategies for networks on chip

Ubar, Raimund-Johannes; Raik, Jaan Networks on chip 2003 / p. 131-152 : ill https://link.springer.com/chapter/10.1007/0-306-48727-6_7

3D parallel fault simulation

Gorev, Maksim; Ubar, Raimund-Johannes Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 39-42 : ill

Timing simulation of digital circuits with binary decision diagrams

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. Design, Automation and Test in Europe : Conference and Exhibition 2001 : Munich, Germany, March 13-16, 2001 : proceedings 2001 / p. 460-466 : ill <https://ieeexplore.ieee.org/document/915063>

True path tracing in structurally synthesized BDDs for testability analysis of digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Oyeniran, Adeboye Stephen; Jenihhin, Maksim Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 492-499 : ill <https://doi.org/10.1109/DSD.2019.00077>

Using constraint solver in Test Pattern Generation Tool

Viilukas, Taavi; Raik, Jaan Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 14-17 : ill

Web-based framework for parallel distributed test [Electronic resource]

Ivask, Eero; Raik, Jaan; Ubar, Raimund-Johannes 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 / p. 271-274 : ill. [CD-ROM] <https://ieeexplore.ieee.org/document/4538800>

Исследование и разработка методов управления поиском дефектов в цифровых схемах : автореферат кандидата технических наук (05.13.01)

Evartson, Teet 1986 https://www.ester.ee/record=b1301665*est

Оценка тенденции использования некоторых видов микросхем

Maltsev, Jüri; Ševtšenko, S. Тезисы докладов республиканской научно-технической конференции, посвященной Дню радио. [1], Секция: Информационно-измерительная техника 1981 / с. 25-26 https://www.ester.ee/record=b1310782~S1*est

Построение полных контролирующих тестов комбинационных схем

Ubar, Raimund-Johannes Eesti NSV Teaduste Akadeemia toimetised. Füüsika. Matemaatika = Известия Академии наук Эстонской ССР. Физика. Математика = Proceedings of Academy of Sciences of the Estonian SSR. Physics. Mathematics 1982 / lk. 418-427; ill. https://www.ester.ee/record=b1264310*est

Построение тестов цифровых схем при помощи модели Альтернативных графов

Plakk, Mari; Ubar, Raimund-Johannes Автоматика и телемеханика 1980 / с. 152-163 : илл https://www.ester.ee/record=b1515055*est

Проектирование контролепригодных дискретных систем : учебное пособие

Ubar, Raimund-Johannes 1988 https://www.ester.ee/record=b1225400*est