

Automated correction of design errors by edge redirection on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan 13th International Symposium on Quality Electronic Design (ISQED), 2012 2012 / p. 686-693 : ill <https://ieeexplore.ieee.org/document/6113980>

Canonical representations of high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Raik, Jaan; Tombak, Mati Estonian journal of engineering 2010 / 1, p. 39-55 : ill

Formal verification and error correction on high-level decision diagrams = Formaalne verifitseerimine ja vigade parandamine kõrgtasemelistel otsustusdiagrammidel

Karputkin, Anton 2012

Generating directed tests for C programs using RTL ATPG

Raik, Jaan; Drenkhan, Tiia; Jenihhin, Maksim; Viilukas, Taavi; Karputkin, Anton; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the IEEE 13th Workshop on RTL and High Level Testing (WRTL'12) 2012 / p. 1-6

High level decision diagrams and characteristic polynomials

Karputkin, Anton Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 143-146 : ill

Identifying untestable faults in sequential circuits using test path constraints

Viilukas, Taavi; Karputkin, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill <https://link.springer.com/article/10.1007/s10836-012-5312-5>

Interactive presentation abstract : automated correction of design errors by edge redirection on high-level decision diagrams [Electronic resource]

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan IEEE International High Level Design Validation and Test Workshop (HLDVT'11), November 9-11, 2011, Napa Valley, CA 2011 / p. 83 : ill. [CD-ROM]
<http://doi.ieeecomputersociety.org/10.1109/HLDVT.2011.6113980>

Probabilistic equivalence checking based on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 423-428 : ill
<https://ieeexplore.ieee.org/document/5783130>

Synthesis of high-level decision diagrams for functional test pattern generation

Ubar, Raimund-Johannes; Raik, Jaan; Karputkin, Anton; Tombak, Mati Proceedings of the 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009 : Lodz, Poland, 25-27 June, 2009 2009 / p. 519-524 : ill

A synthesis-agnostic behavioral fault model for high gate-level fault coverage

Karputkin, Anton; Raik, Jaan 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2016 / p. 1124-1127 : ill <https://ieeexplore.ieee.org/document/7459477/figures#figures>

Verification and error correction on High-Level Decision Diagrams

Karputkin, Anton 2013