

Challenges of reliability assessment and enhancement in autonomous systems

Jenihhin, Maksim; Sonza Reorda, Matteo; **Balakrishnan, Aneesh**; Alexandrescu, Dan 2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2019) 2019 / 6 p <https://doi.org/10.1109/DFT.2019.8875379>

Composing graph theory and deep neural networks to evaluate SEU type soft error effects

Balakrishnan, Aneesh; Lange, Thomas; Glorieux, Maximilien; Alexandrescu, Dan; **Jenihhin, Maksim** 9th Mediterranean Conference on Embedded Computing (MECO'2020), Budva, Montenegro, 8-11 June 2020 2020
<https://doi.org/10.1109/MECO49872.2020.9134279>

Enabling cross-layer reliability and functional safety assessment through ML-based compact models

Alexandrescu, Dan; **Balakrishnan, Aneesh**; Lange, Thomas; Glorieux, Maximilien Proceedings : 2020 26th IEEE International Symposium on On-Line Testing and Robust System Design : IOLTS 2020, Napoli, Italy, July 13-16, 2020 : virtual edition 2020 / 6 p. : ill <https://doi.org/10.1109/IOLTS50870.2020.9159750>

Gate-level graph representation learning : a step towards the improved stuck-at faults analysis

Balakrishnan, Aneesh; Alexandrescu, Dan; **Jenihhin, Maksim**; Lange, Thomas; Glorieux, Maximilien Proceedings of the Twenty Second International Symposium on Quality Electronic Design (ISQED) : Santa Clara, USA, 7-9 April 2021 2021 / p. 24-30
<https://doi.org/10.1109/ISQED51717.2021.9424256>

Machine learning clustering techniques for selective mitigation of critical design features

Lange, Thomas; **Balakrishnan, Aneesh**; Glorieux, Maximilien; Alexandrescu, Dan; Sterpone, Luca Proceedings : 2020 26th IEEE International Symposium on On-Line Testing and Robust System Design : IOLTS 2020, Napoli, Italy, July 13-16, 2020 : virtual edition 2020 / 7 p. : ill <https://doi.org/10.1109/IOLTS50870.2020.9159751>

Machine learning to tackle the challenges of transient and soft errors in complex circuits

Lange, Thomas; **Balakrishnan, Aneesh**; Glorieux, Maximilien; Alexandrescu, Dan; Sterpone, Luca 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS), 1-3 July 2019, Greece 2019 / p. 7-14 : ill
<https://doi.org/10.1109/IOLTS.2019.8854423>

Modeling gate-level abstraction hierarchy using graph convolutional neural networks to predict functional de-rating factors

Balakrishnan, Aneesh; Lange, Thomas; Glorieux, Maximilien; Alexandrescu, Dan; **Jenihhin, Maksim** 2019 NASA/ESA conference on adaptive hardware and systems AHS 2019 : proceedings 2019 / p. 72-78 : ill <https://doi.org/10.1109/AHS.2019.00007>

Modeling soft-error reliability under variability

Balakrishnan, Aneesh; Cardoso Medeiros, Guilherme; Gürsoy, Cemil Cem; Hamdioui, Said; **Jenihhin, Maksim**; Alexandrescu, Dan 2021 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 6-8 Oct. 2021 2021 / p. 1-6 <https://doi.org/10.1109/DFT52944.2021.9568295>

On antagonism between side-channel security and soft-error reliability in BNN inference engines

Lai, Xinhui; Lange, Thomas; **Balakrishnan, Aneesh**; Alexandrescu, Dan; **Jenihhin, Maksim** IFIP/IEEE 29th International Conference on Very Large Scale Integration (VLSI-SoC) 2021 / p. 1-6 <https://doi.org/10.1109/VLSI-SoC53125.2021.9606981>

On the estimation of complex circuits functional failure rate by machine learning techniques

Lange, Thomas; **Balakrishnan, Aneesh**; Glorieux, Maximilien; Alexandrescu, Dan; Sterpone, Luca 49th Annual IEEE/IFIP International Conference on Dependable Systems and Networks - DSN 2019 : Supplemental Volume : proceedings 2019 / p. 35-41 : ill <https://doi.org/10.1109/DSN-S.2019.00021>

A synthetic, hierarchical approach for modelling and managing complex systems' quality and reliability = Sünteetiline, hierarhiline lähenemine keerukate süsteemide kvaliteedi ja töökindluse modelleerimiseks ja haldamiseks

Balakrishnan, Aneesh 2022 <https://doi.org/10.23658/taltech.11/2022> <https://digikogu.taltech.ee/et/Item/a594d3ec-0e6b-4a78-819a-fe1f47992612>

The validation of graph model-based, gate level low-dimensional feature data for machine learning applications

Balakrishnan, Aneesh; Lange, Thomas; Glorieux, Maximilien; Alexandrescu, Dan; **Jenihhin, Maksim** 2019 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC), 29-30 October 2019, Helsinki, Finland : proceedings in IEEE Xplore 2019 / 7 p <https://doi.org/10.1109/NORCHIP.2019.8906974>

Understanding multidimensional verification : where functional meets non-functional

Lai, Xinhui; **Balakrishnan, Aneesh**; Lange, Thomas; **Jenihhin, Maksim**; Ghasempouri, Tara; Raik, Jaan; Alexandrescu, Dan Microprocessors and microsystems 2019 / art. 102867, 13 p. : ill <https://doi.org/10.1016/j.micpro.2019.102867> [Journal metrics at Scopus](#)
[Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)