

Defect-oriented test- and layout-generation for standard-cell ASIC designs

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Deterministic defect-oriented test generation for combinational circuits

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DOT: new deterministic defect-oriented ATPG tool

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Hierarchical analysis of short defects between metal lines in CMOS IC

Pleskacz, Witold A.; **Jenihhin, Maksim; Raik, Jaan**; Rakowski, Michal; **Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw Proceedings : 11th EUROMICRO Conference on Digital System Design : Architectures, Methods and Tools : (DSD 2008) : September 3-5, 2008, Parma, Italy 2008 / p. 729-734 : ill

Module level defect simulation in digital circuits

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